

Handout 8: Lead compensation

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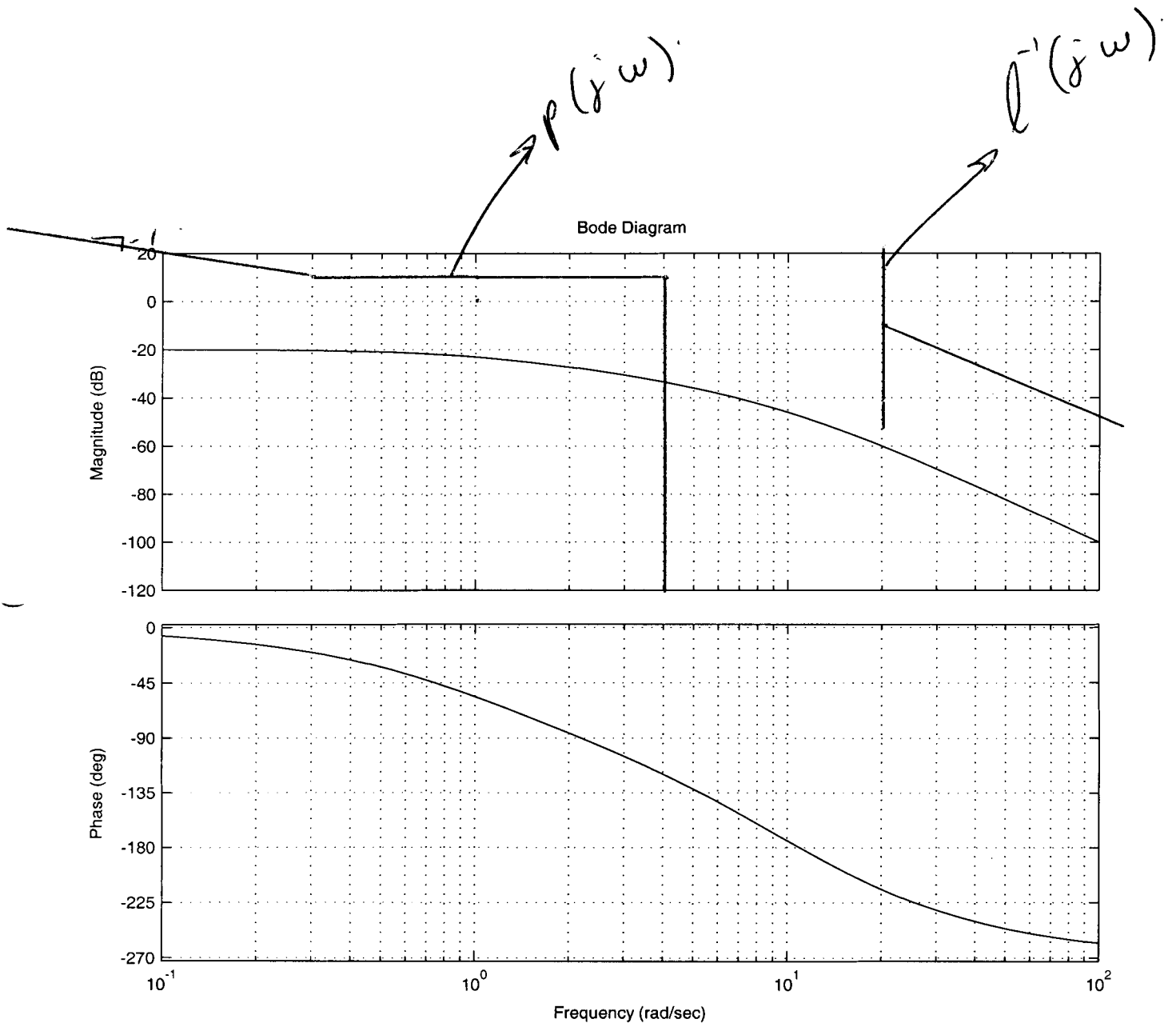
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Lead Compensation goals: Raise phase (and gain) at high frequencies while not touching low-frequency system's characteristics: Can extend *bandwidth* of system.

Canonical lead element:

$$K_{lead}(s) = \frac{s/a + 1}{s/b + 1}, \quad 0 \leq a < b.$$

Typical lead Bode Plot:



$$K_p = 110$$

Using Lead-Lag / PID compensation

Plant under study:

$$G(s) = \frac{1/10}{(s+1)(s/10+1)^2}$$

‘ Requirements: Want to have good tracking ($p(j\omega)$), insensitivity to high frequency unmodelled dynamics ($l(j\omega)$), decent PM.

Compensation Scheme: We first adjust the gain K in the feedback loop to 110.

Phase Margin is

Gain Margin is

BW is

Lead compensation:

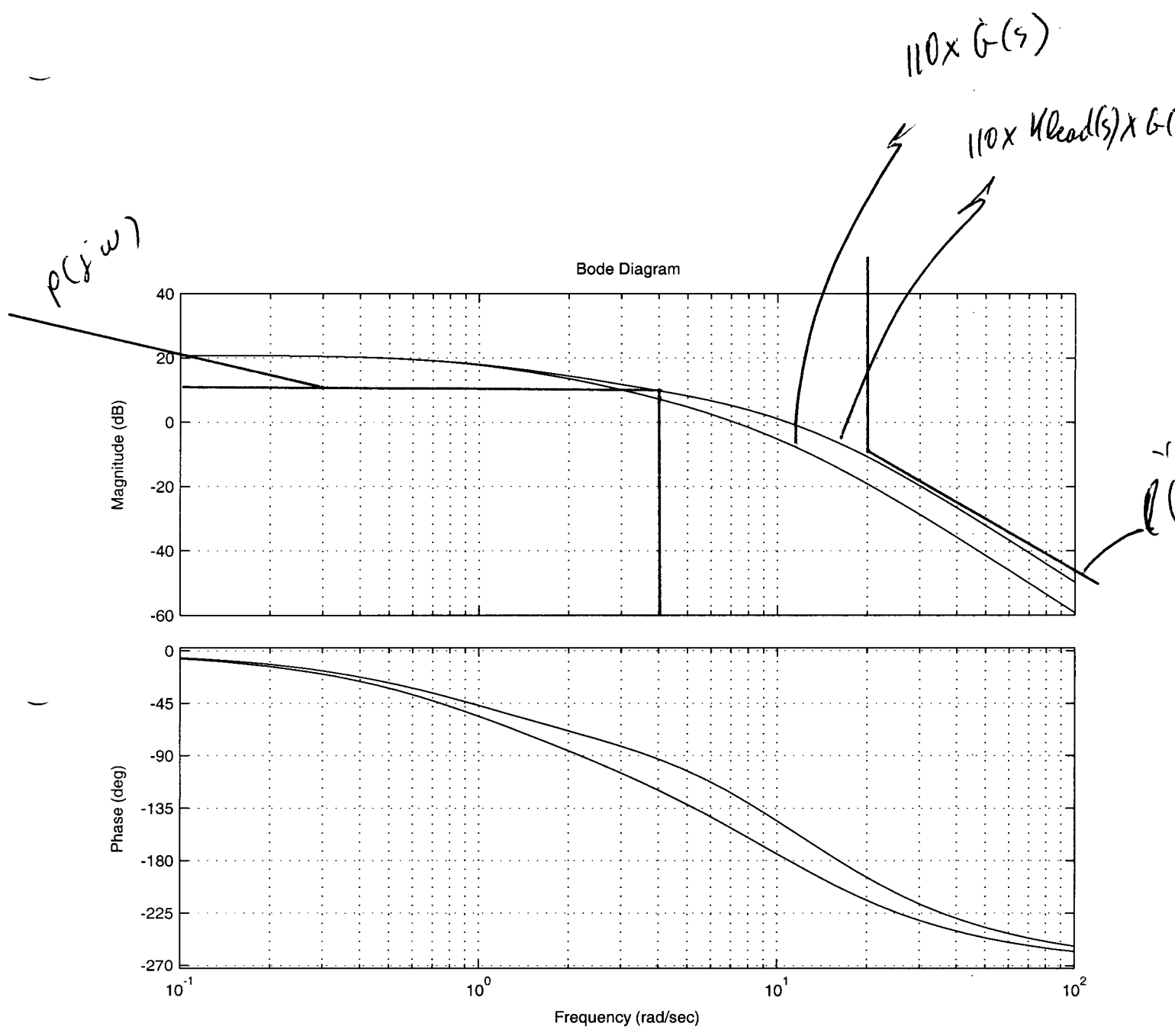
$$K_{lead}(s) = \frac{s/c + 1}{s/d + 1}$$

Lag compensation:

$$K_{lag}(s) = \frac{s + a}{s + b}$$

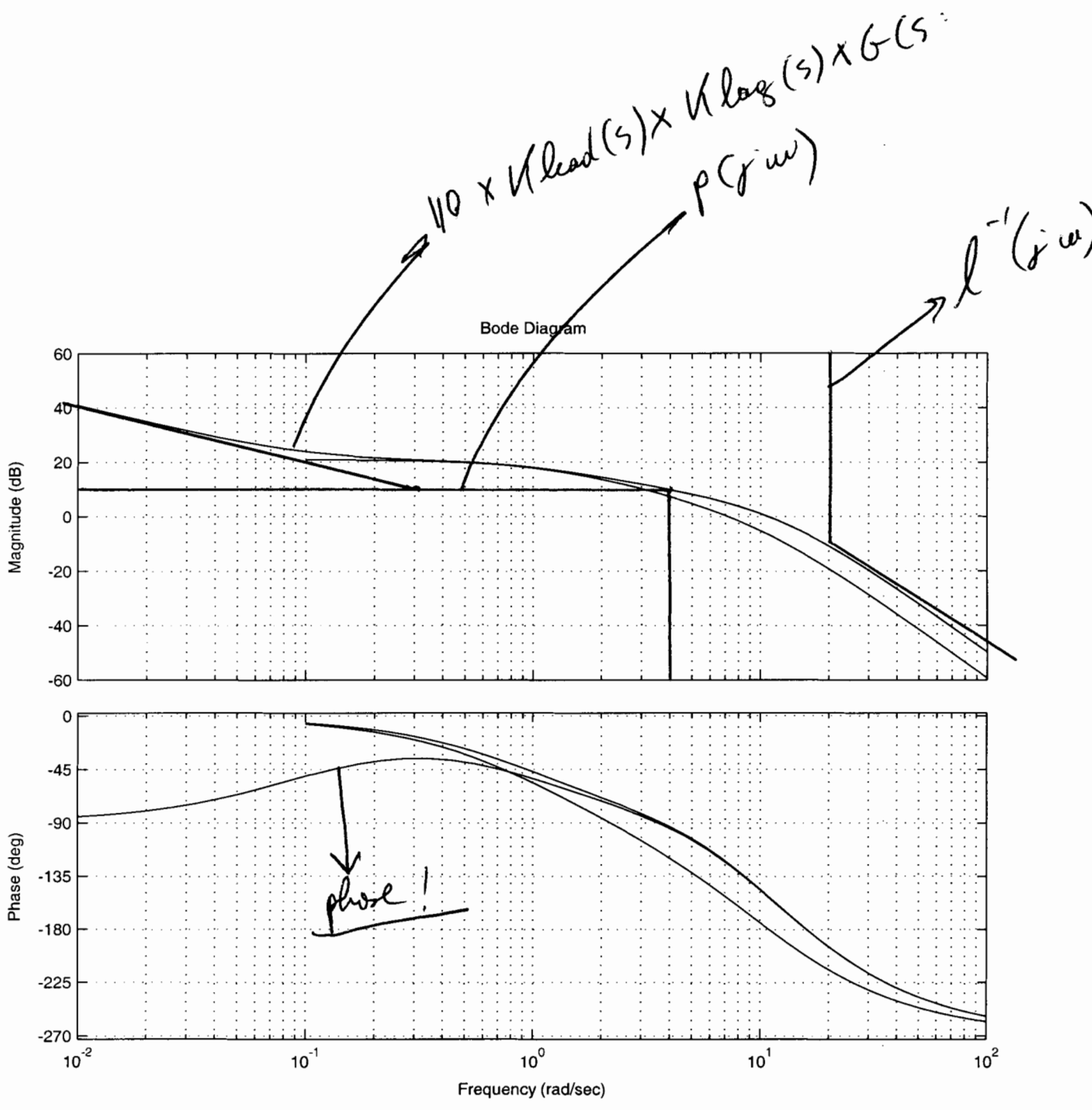
Final design: Bode plot

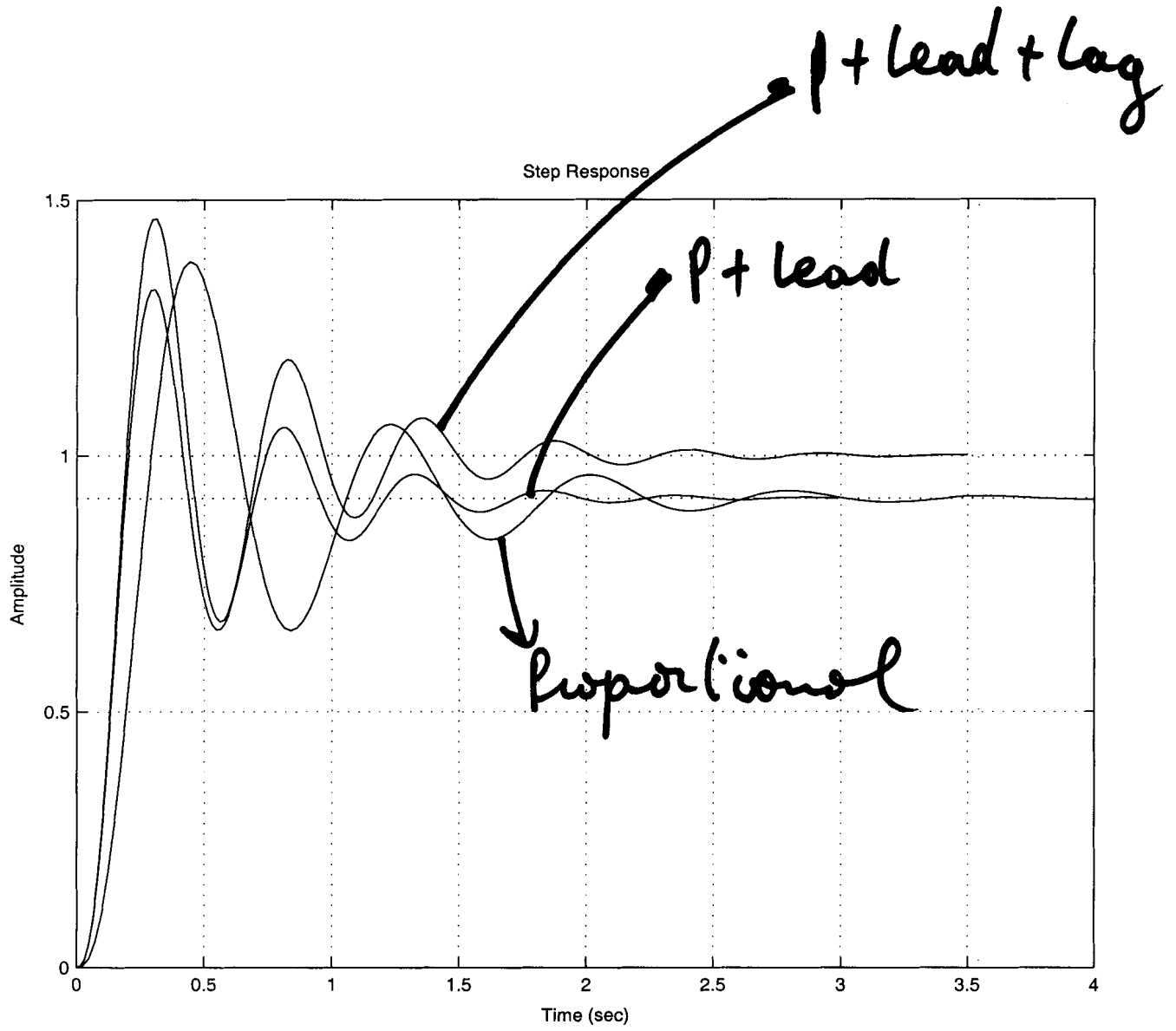
Final design: Root locus



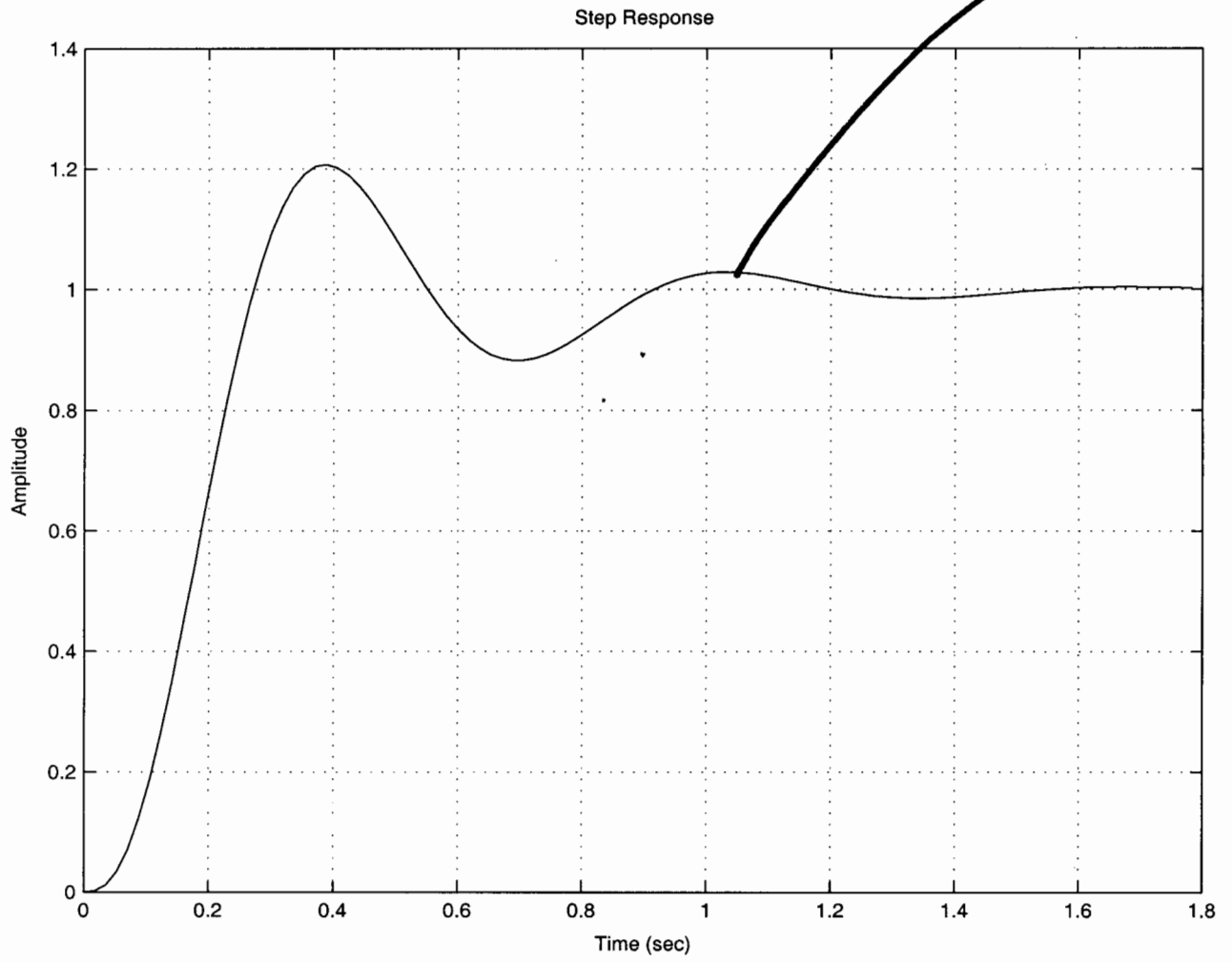
$$d = 12$$

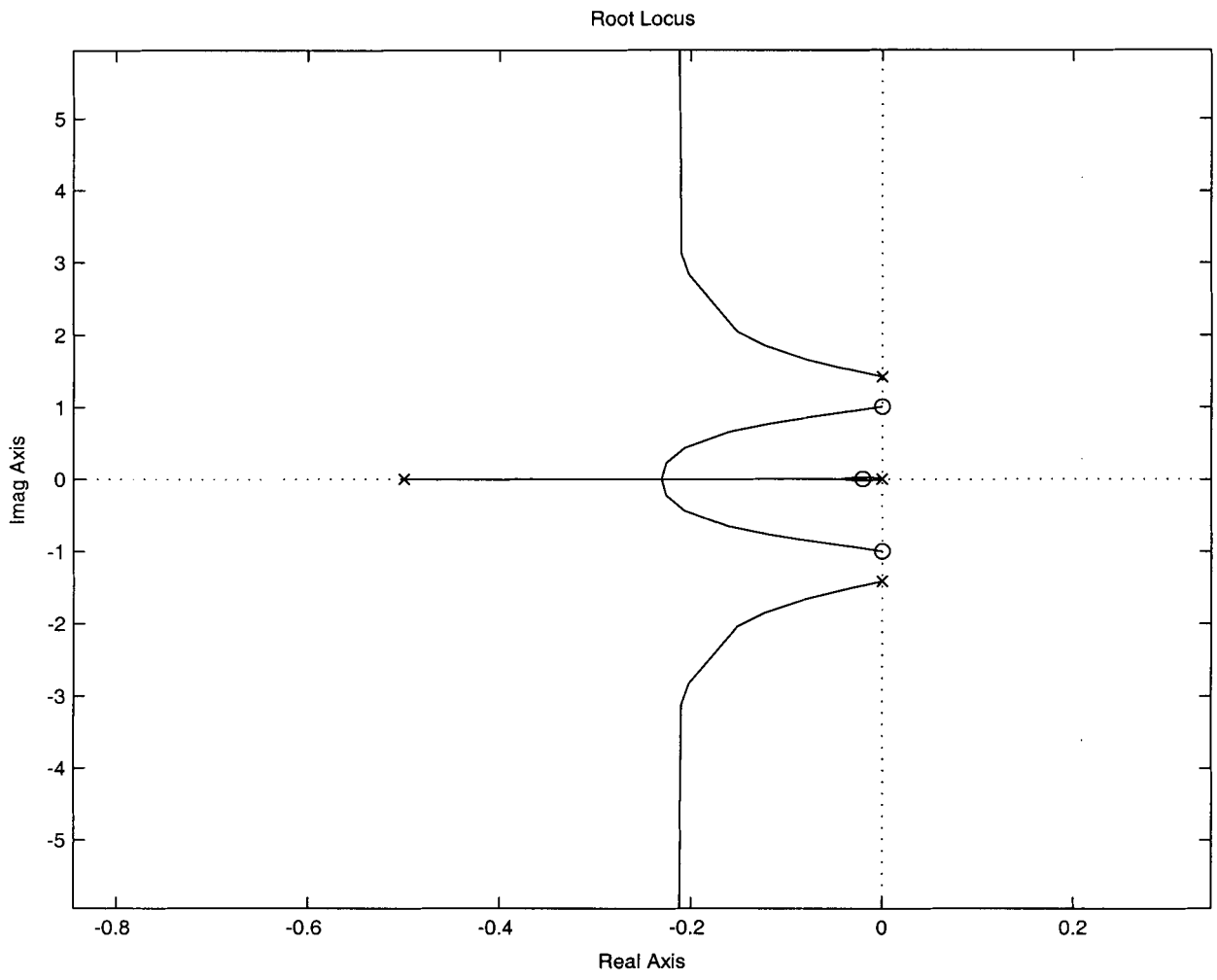
$$c = 4$$



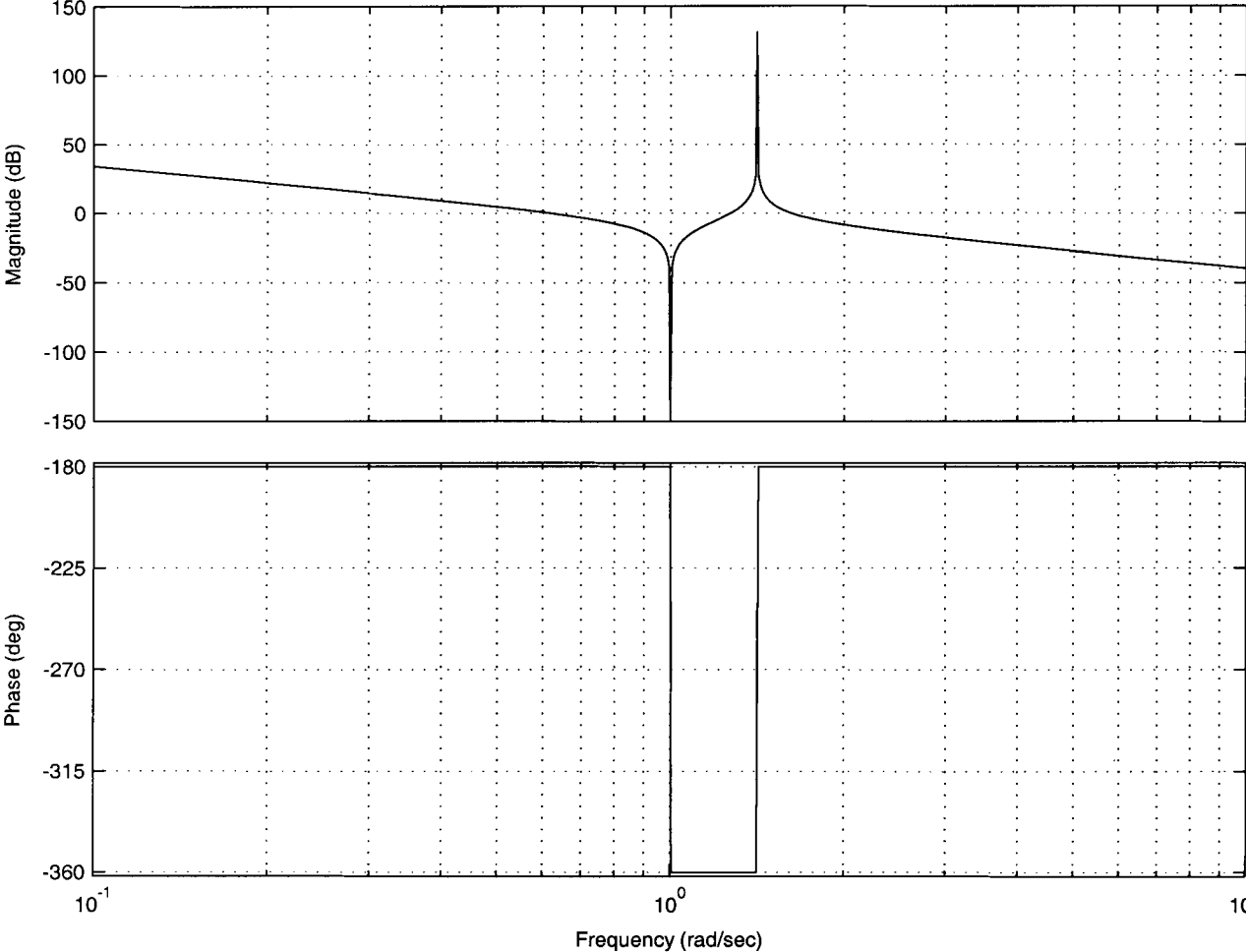


$K: 110 \rightarrow 66$

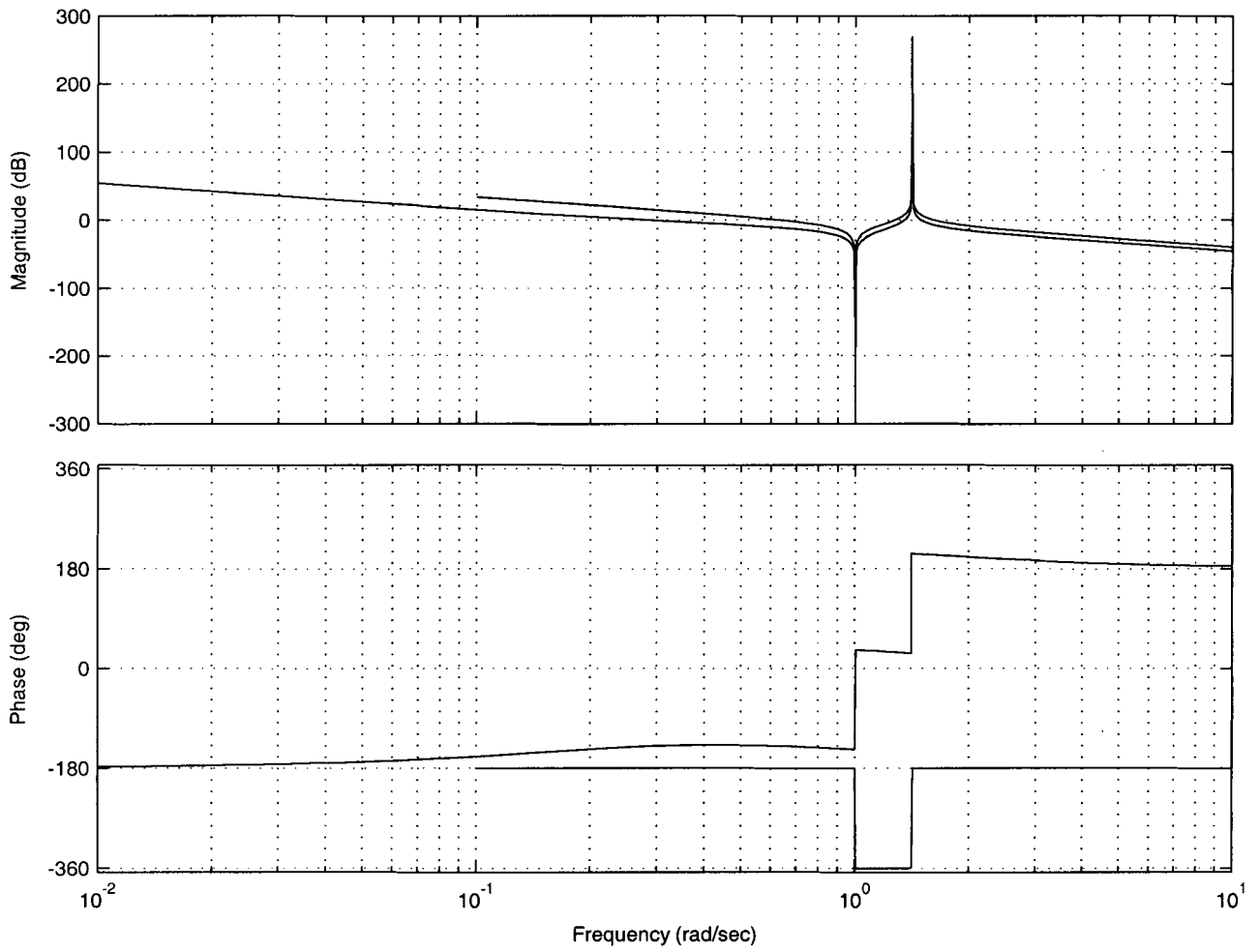




Bode Diagram



Bode Diagram



~~0.2~~ $\frac{s/0.02 + 1}{s/2 + 1}$

$K = 0.2$