Lecture 7 - PN Junction and MOS Electrostatics (IV)

ELECTROSTATICS OF METAL-OXIDE-SEMICONDUCTOR STRUCTURE

September 29, 2005

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Reading assignment:

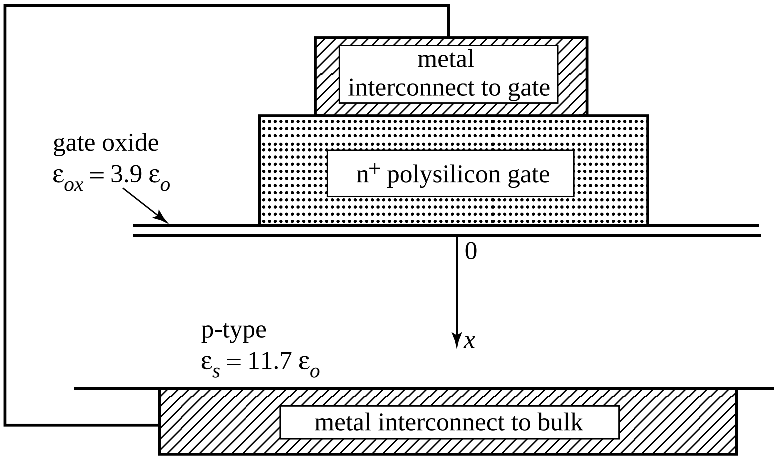
Howe and Sodini, Ch. 3, §§3.7-3.8

Key questions

- What is the big deal about the metal-oxide-semiconductor structure?
- What do the electrostatics of the MOS structure look like at zero bias?
- How do the electrostatics of the MOS structure get modified if a voltage is applied across its terminals?

1. Introduction

Metal-Oxide-Semiconductor structure:

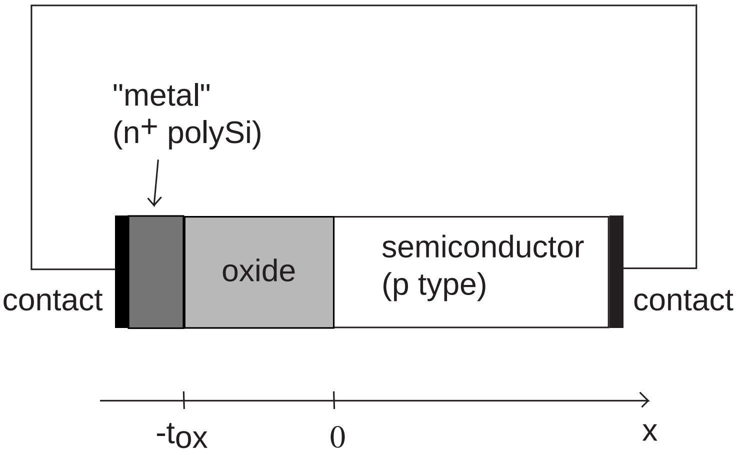


MOS at the heart of the electronics revolution:

- *Digital and analog functions*: Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is key element of Complementary Metal-Oxide-Semiconductor (CMOS) circuit family
- *Memory function*: Dynamic Random Access Memory (DRAM) and Flash Erasable Programmable Memory (EPROM)
- *Imaging*: Charge-Couple Device (CCD) camera, also CMOS imagers
- *Displays*: Active-Matrix Liquid-Crystal Displays
- ...

2. MOS electrostatics at zero bias

Idealized 1D structure:



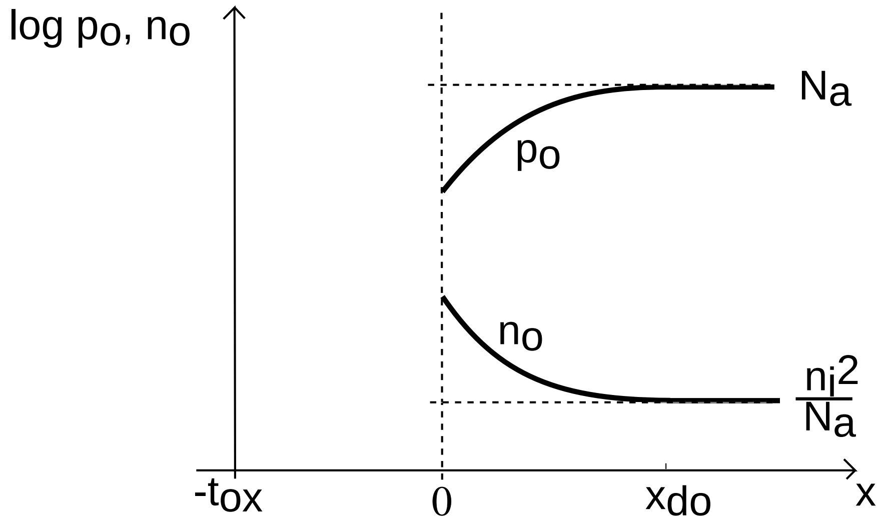
- Metal: does not tolerate volume charge ⇒ charge can only exist at its surface
- Oxide: insulator ⇒ no volume charge (no free carriers, no dopants), it does not conduct
- Semiconductor: can have volume charge (SCR)

Thermal equilibrium can't be established through oxide; need wire to allow transfer of charge between metal and semiconductor. → refer to this as zero bias

MOS structure: sandwich of dissimilar materials ⇒ carrier transfer ⇒ space-charge region at zero bias ⇒ built-in potential

What does the electrostatics picture look like?

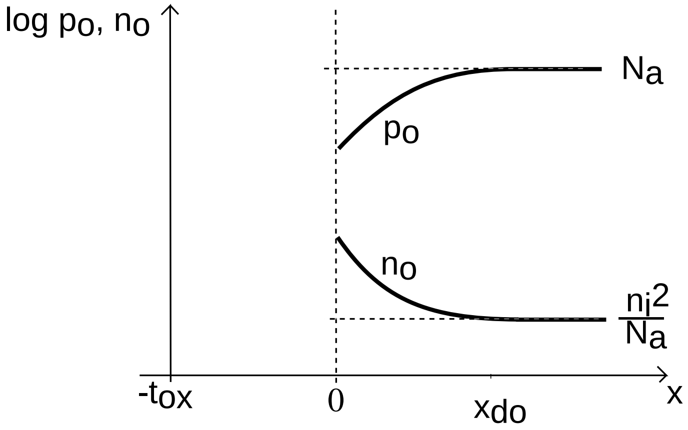
For most metals on p-Si, equilibrium achieved by electrons diffusing from metal to semiconductor and holes from semiconductor to metal:

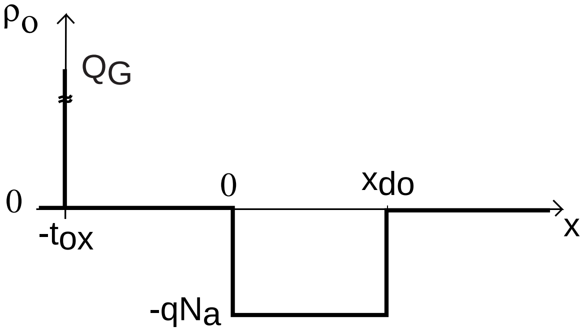


Remember: $n_o p_o = n_i^2$

Fewer holes near Si/SiO$_2$ interface ⇒ ionized acceptors exposed (volume space charge)

□ SPACE CHARGE DENSITY





- In semiconductor: space-charge region close to Si/SiO_2 interface ⇒ can do *depletion approximation*
- In metal: sheet of charge at metal/SiO_2 interface
- Overall charge neutrality

C/cm²

$$\begin{array}{rcll} x & \le & -t_{ox} & \rho_o(x) = Q_G\,\delta(-t_{ox}) \\ -t_{ox} & < & x < 0 & \rho_o(x) = 0 \\ 0 & < & x < x_{do} & \rho_o(x) = -qN_a \\ x_{do} & < & x & \rho_o(x) = 0 \end{array}$$

C/cm³

□ ELECTRIC FIELD

Integrate Gauss' equation:

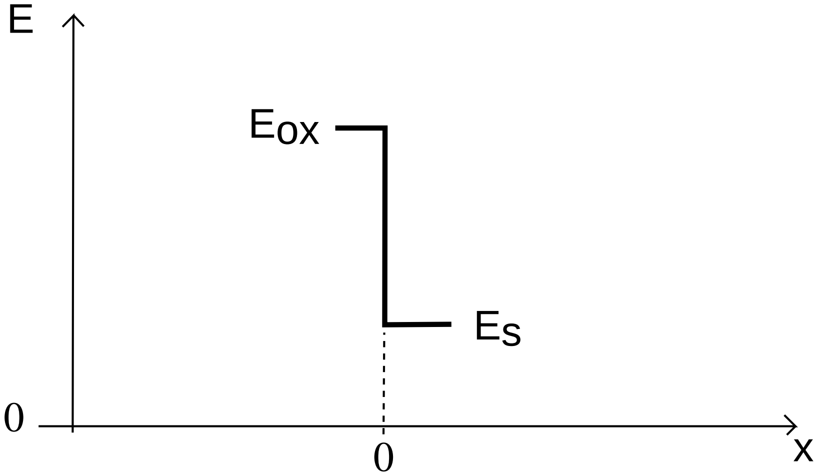
$$E_o(x_2) - E_o(x_1) = \frac{1}{\epsilon}\int_{x_1}^{x_2} \rho_o(x)dx$$

At interface between oxide and semiconductor:

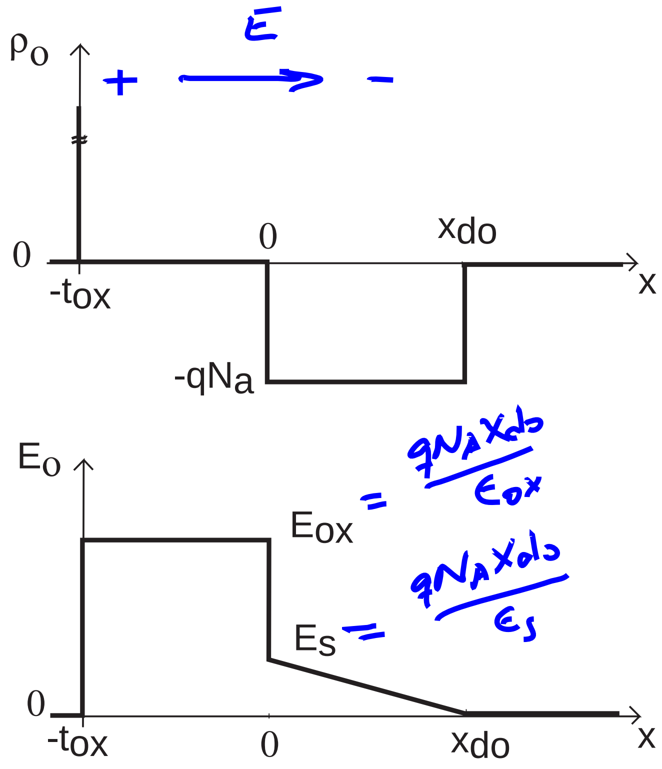
change in permittivity ⇒ change in electric field

$$\epsilon_{ox}E_{ox} = \epsilon_s E_s$$

$$\boxed{\frac{E_{ox}}{E_s} = \frac{\epsilon_s}{\epsilon_{ox}} \simeq 3}$$



Start integrating from deep inside semiconductor:



$$x_{do} < x \qquad E_o(x) = 0$$

$$0 < x < x_{do} \qquad E_o(x) = -\frac{qN_a}{\epsilon_s}(x - x_{do})$$

$$-t_{ox} < x < 0 \qquad E_o(x) = \frac{\epsilon_s}{\epsilon_{ox}} E_o(x = 0^+) = \frac{qN_a x_{do}}{\epsilon_{ox}}$$

$$x < -t_{ox} \qquad E_o(x) = 0$$

☐ ELECTROSTATIC POTENTIAL

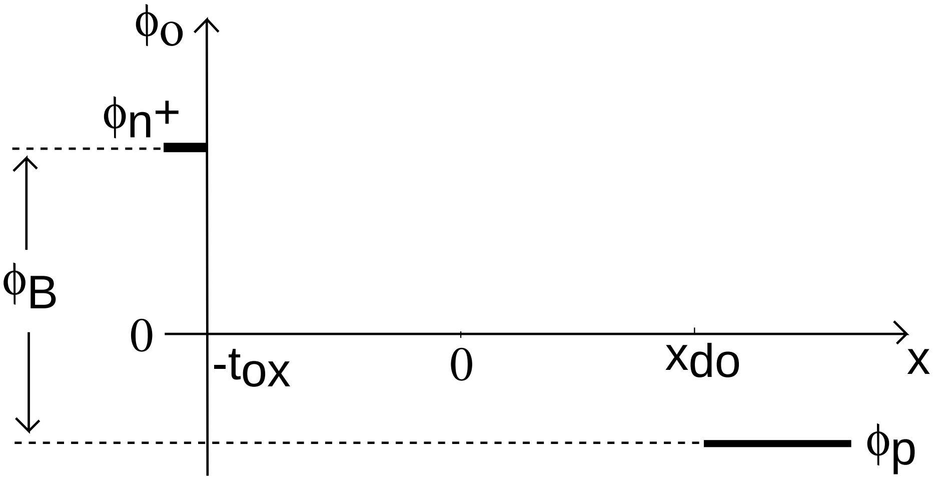
(with $\phi = 0$ @ $n_o = p_o = n_i$)

$$\phi = \frac{kT}{q} \ln \frac{n_o}{n_i} \qquad \phi = -\frac{kT}{q} \ln \frac{p_o}{n_i}$$

In QNR's, n_o and p_o known ⇒ can determine ϕ:

in n^+ gate: $n_o = N_d^+ \ \Rightarrow \ \phi_g = \phi_{n^+}$

in p-QNR: $p_o = N_a \ \Rightarrow \ \phi_p = -\frac{kT}{q} \ln \frac{N_a}{n_i}$

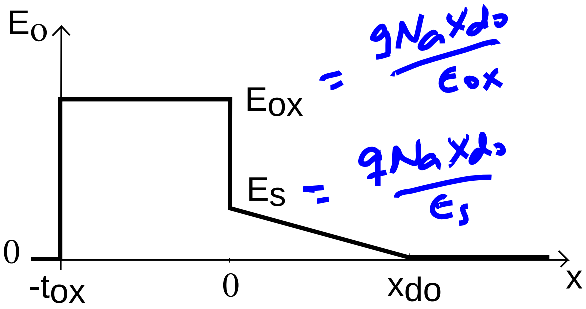


Built-in potential:

$$\boxed{\phi_B = \phi_g - \phi_p = \phi_{n^+} + \frac{kT}{q} \ln \frac{N_a}{n_i}}$$

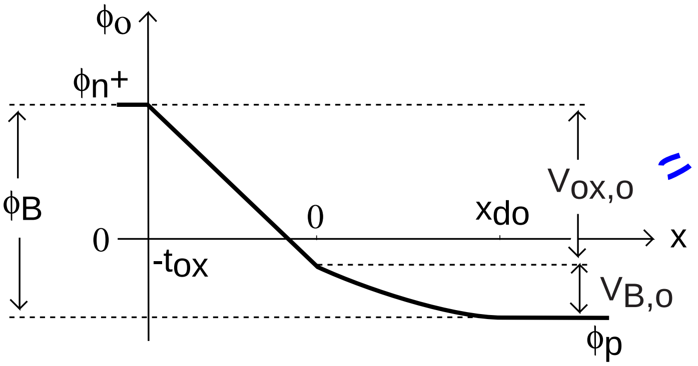
To get $\phi_o(x)$, integrate $E_o(x)$; start from deep inside semiconductor bulk:

$$\phi_o(x_2) - \phi_o(x_1) = -\int_{x_1}^{x_2} E_o(x)dx$$



$E_{ox} = \frac{qN_a x_{do}}{\epsilon_{ox}}$

$E_s = \frac{qN_a x_{do}}{\epsilon_s}$



$V_{ox,o} = E_{ox} t_{ox} = \frac{qN_a x_{do} t_{ox}}{\epsilon_{ox}}$

$V_{B,o} = \frac{qN_a x_{do}^2}{2\epsilon_s}$

$$x_{do} < x \qquad \phi_o(x) = \phi_p$$

$$0 < x < x_d \qquad \phi_o(x) = \phi_p + \frac{qN_a}{2\epsilon_s}(x - x_{do})^2$$

$$-t_{ox} < x < 0 \qquad \phi_o(x) = \phi_p + \frac{qN_a x_{do}^2}{2\epsilon_s} + \frac{qN_a x_{do}}{\epsilon_{ox}}(-x)$$

$$x < -t_{ox} \qquad \phi_o(x) = \phi_{n^+}$$

□ Still don't know x_{do} ⇒ need one more equation:

Potential difference across structure has to add up to ϕ_B:

$$\phi_B = V_{B,o} + V_{ox,o} = \frac{qN_a x_{do}^2}{2\epsilon_s} + \frac{qN_a x_{do} t_{ox}}{\epsilon_{ox}}$$

Solve quadratic equation:

$$x_{do} = \frac{\epsilon_s}{\epsilon_{ox}} t_{ox} [\sqrt{1 + \frac{2\epsilon_{ox}^2 \phi_B}{\epsilon_s q N_a t_{ox}^2}} - 1] = \frac{\epsilon_s}{C_{ox}} [\sqrt{1 + \frac{4\phi_B}{\gamma^2}} - 1]$$

where C_{ox} is *capacitance per unit area of oxide* [units: F/cm^2]:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

and γ is *body factor coefficient* [units: $V^{\overset{\swarrow}{+}1/2}$]:

$$\gamma = \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_a}$$

☐ Numerical example:

$$N_d = 10^{20}\ cm^{-3},\ N_a = 10^{17}\ cm^{-3},\ t_{ox} = 8\ nm$$

$$\phi_B = 550\ mV + 420\ mV = 970\ mV$$

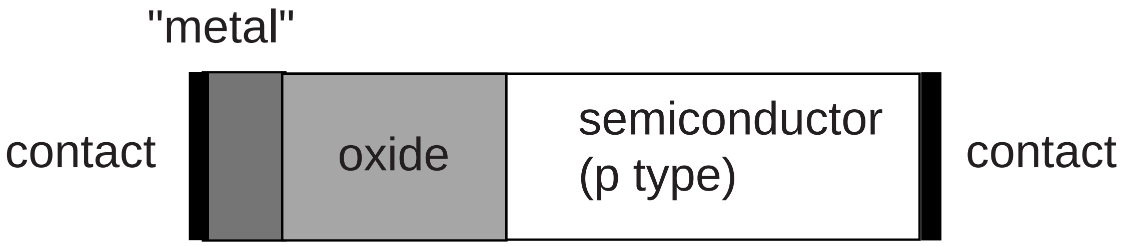
$$C_{ox} = 4.3 \times 10^{-7}\ F/cm^2$$

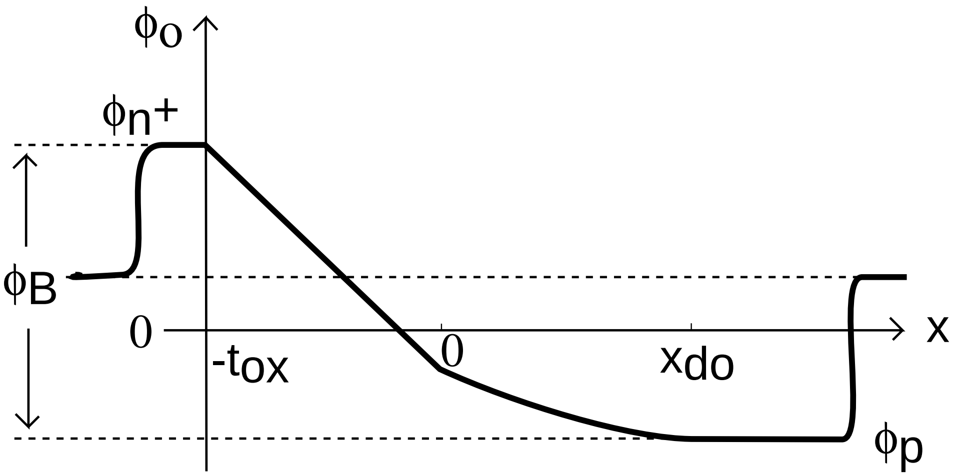
$$\gamma = 0.43\ V^{1/2}$$

$$x_{do} = 91\ nm$$

There are also *contact potentials*

⇒ total contact-to-contact potential difference is zero!





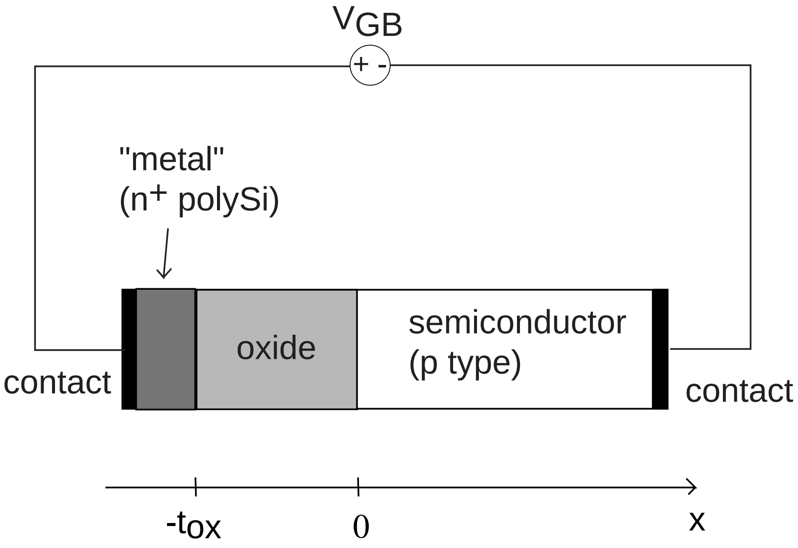
picture consistent:

- need negative charge in semiconductor and positive charge at metal/SiO_2 interface to justify potential distribution ⇒

⇒ need depletion region

3. MOS electrostatics under bias

Apply voltage to gate with respect to semiconductor:



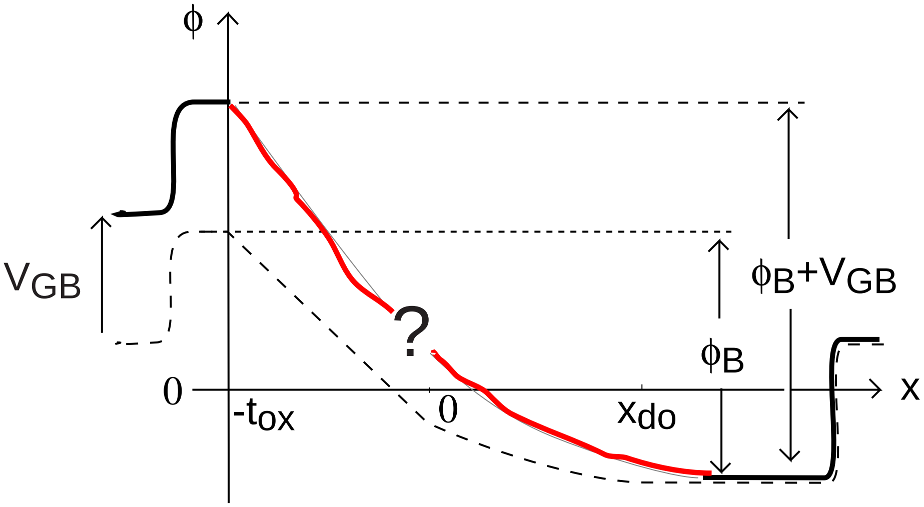
Electrostatics of MOS structure affected ⇒ potential difference across entire structure now $\neq 0$.

How is potential difference accommodated?

Potential can drop in:

- gate contact
- n^+-polysilicon gate
- oxide
- semiconductor SCR
- semiconductor QNR
- semiconductor contact

Potential difference shows up across oxide and SCR in semiconductor:

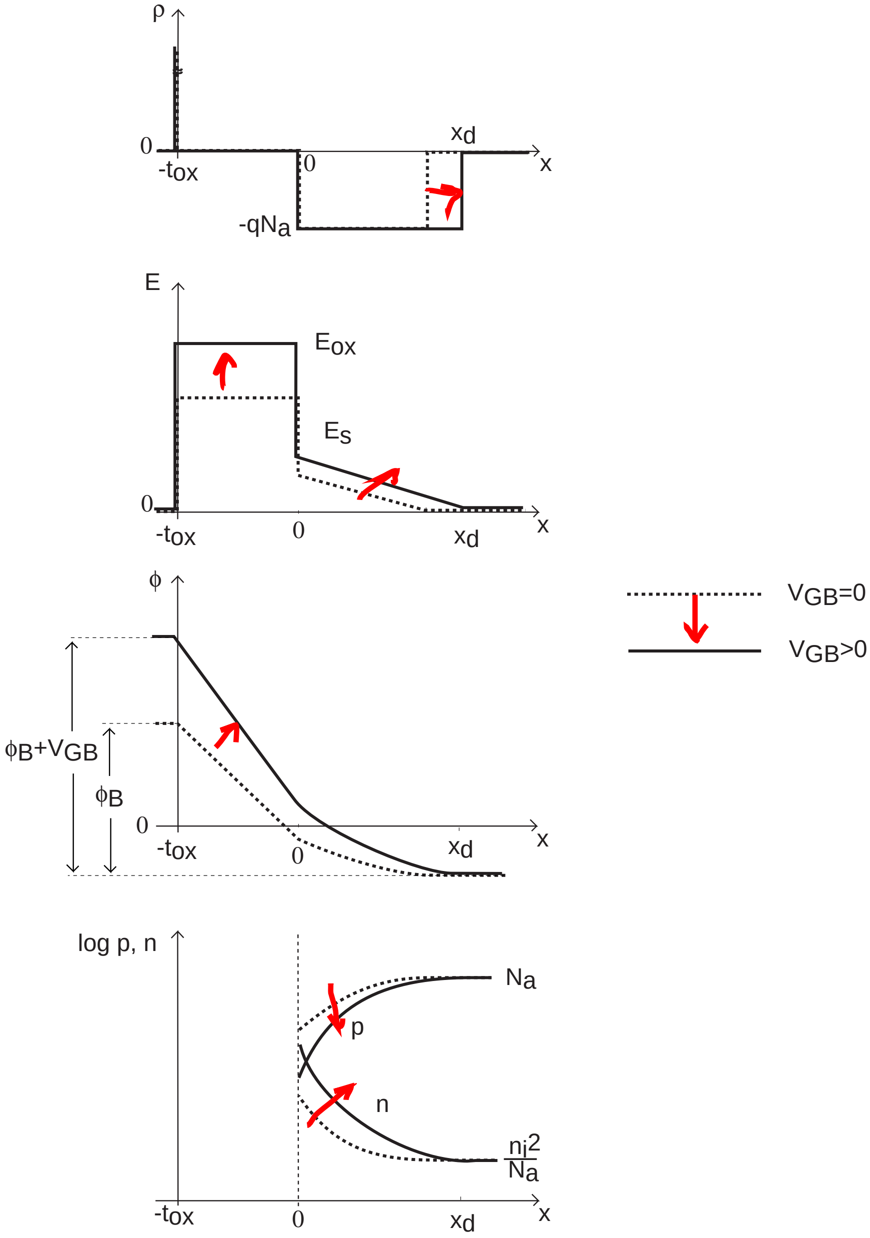


Oxide is insulator ⇒ no current anywhere in structure

In SCR, quasi-equilibrium situation prevails
⇒ new balance between drift and diffusion

- electrostatics qualitatively identical to zero bias (but *amount of charge redistribution is different*)
- $np = n_i^2$

Apply $V_{GB} > 0$: potential difference across structure increases ⇒ need larger charge dipole ⇒ SCR expands into semiconductor substrate:



Simple way to remember:

with $V_{GB} > 0$, gate attracts electrons and repels holes.

Qualitatively, physics unchanged by applying $V_{GB} > 0$.

Use mathematical formulation of zero bias, but:

$$\phi_B \rightarrow \phi_B + V_{GB}$$

For example,

$$x_d(V_{GB}) = \frac{\epsilon_s}{C_{ox}}[\sqrt{1 + \frac{4(\phi_B + V_{GB})}{\gamma^2}} - 1]$$

$$V_{GB} \uparrow \rightarrow \ x_d \uparrow$$

Key conclusions

- Charge redistribution in MOS structure at zero bias:
  - SCR in semiconductor
  - built-in potential across MOS structure.
- In most cases, can do depletion approximation in semiconductor SCR.
- Application of voltage modulates depletion region width in semiconductor. No current flows.