# DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE **MASSACHUSETTS INSTITUTE OF TECHNOLOGY** CAMBRIDGE. MASSACHUSETTS 02139

## Spring Term 2007 6.101 Introductory Analog Electronics Laboratory Laboratory No. 5

# READING ASSIGNMENT

Horowitz and Hill: The Art of Electronics, pp. 91-94, pp. 98-101, pp.286-288 Neamen 2<sup>nd</sup> Edition: pp. 499-502, pp. 484 [8.3.2] – 491 top Neamen 3<sup>rd</sup> Edition: pp. 593-596, pp. 578 [8.3.2] – 586 top

<u>Objective</u>: Build a small audio power amp and play loud music! Study the differential amplifier, the heart of most op-amps. Play with the ubiquitous 555-timer chip. <u>NOTE</u>: Your lab write-up should <u>clearly</u> show your circuit configurations, your element values and your calculations in addition to measurement results. The grader will not spend time trying to sift through messy presentations to find out what you did. <u>NOTE: THIS LAB REQUIRES A CHECKOFF FOR EXPERIMENT ONE. Sign up</u> for your checkoff time on the list posted on the lab door.

Experiment 1: SMALL POWER AMPLIFIER WITH LOCAL AND OVERALL FEEDBACK

NOTE: Do not use the variable power supply terminals on your kit for this experiment. The output current from these terminals is limited to 500 mA, and this is too low for this amplifier when driving a loudspeaker. Use the +/- 12 volt fixed terminals next to the power switch. These terminals can deliver 1 ampere before they start to current-limit. Even better, you can use the new adjustable power supplies on the lab benches. There are nine of them. First, prove your circuit using the kit variable +/- 15 volt power supplies, then, hook it up to the adjustable supplies [set for +/- 15 volts], hook up a speaker, and enjoy!

NOTE: These adjustable supplies have very large filter capacitors, and they take a while to discharge after the power switch is turned off, if your circuit doesn't draw much current. You may want to monitor the supply voltages with your DMM, and you can also place a "bleeder" resistor across the power supplies' terminals to increase the speed of the capacitor discharge [time constant]. Be careful to choose a resistor with a safe power rating!

In this experiment you will build and examine the performance of the dc-coupled amplifier whose schematic outline is given in Figure 1. This amplifier is intended to have a gain of 20 dB with less distortion than that found in the amplifier of experiment 5 of Lab 4.

• Note that the function of resistors R<sub>B1</sub>, R<sub>B2</sub> and the 1N914 diodes is to bias the output transistors slightly on to eliminate crossover distortion. [Q 1.1 How does this work?] [Use 4.7 kΩ 1/4-watt resistors for R<sub>B1</sub> and R<sub>B2</sub>, at least to start.] In order to ensure that the output transistors Q<sub>1</sub> and Q<sub>2</sub> are not damaged make sure that the maximum power that they will have to dissipate is limited to 1.0 watt. Note that this calculation will involve both the DC power dissipated due to static quiescent current, plus each transistor sees one-half of the output sine wave. Q 1.2 What is the smallest value of load resistance R<sub>L</sub> that can be connected to the output of the amplifier to

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### ensure that this power dissipation limit is not exceeded?

 Note also that the requirement for relatively high input impedance may conflict with the requirement for low DC offset voltage. Q 1.3 Explain this conflict in your write-up. You may choose to use either the inverting or non-inverting configuration for the op-amp. You may choose to use any op-amp available in your kit or at the instrument room window or in the lab drawers.

Q 1.4 What is the function of the emitter resistors  $R_E$ ? Q 1.5 Explain why the output impedance of the amplifier is not at least 5.6  $\Omega$ . [These resistors are in your parts kit and are the larger 1/2-watt size.]

1. Design your amplifier to meet the following specifications:



Figure 1: Amplifier circuit for experiment 1.

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- Input impedance (as seen by preamplifier output) ≥ 20 kΩ. [To prevent loading down of preamps with relatively high source impedance]
- Output stage offset voltage < 50 mV.</li>
   [To keep DC from causing the speaker coil to heat and the cone to be offset from its center position between the magnet pole pieces.]
- High frequency cutoff [-3dB] point = 25 kHz *minimum*.
   [To take advantage of extended high frequency response from DVD audio discs running at 48 kHz sampling rate; also some high-end sound cards.]
- Mid-frequency [1000 Hz] voltage gain of +20 dB.
- Output stage guiescent bias current between 1 and 10 mA [class AB or B operation]. [Measure the DC voltage drop across one or both emitter resistors.] Since we gave you the biasing resistor initial values, there is not much to design. However, you should measure the bias current in the output stages to make sure it is less than 10 mA. Output device  $\beta_{\rm F}$  variations will affect the value of bias current, and it will be hard to achieve a stable bias current if the  $\beta_{\rm F}$ 's of both output devices aren't about the same. If your output device bias current is greater than 10 mA with no signal input, turn off your +/- 12-volt supplies immediately. Increase the value of both R<sub>B1</sub> and R<sub>B2</sub> to the same next highest standard value and recheck the output bias. Keep increasing the value of this pair of resistors until the bias current drops to the limits given above. Q 1.6 How does changing the value of these two resistors control the output stage bias current? [Note: It is also possible to increase these two resistors to the point where not enough DC bias current is supplied to the base of one of the output transistors, especially if it has low  $\beta_{F}$ . It helps if your output devices have similar  $\beta_{\rm F}$ 's. From an AC point of view, large values of these two resistors can cause clipping on one-half cycle due to the fact that not enough AC base current is supplied through these resistors on large signal swings. This is also more likely to occur when the  $\beta_{F}$ 's or  $\beta_{O}$ 's of the two output devices are not equal.] The value of DC bias current is very temperature sensitive and will be higher after you have heated the output devices by amplifying an AC signal. Wait for the devices to cool before measuring the bias current.

Keeping DC bias low prevents wasting power during no-signal periods and heating of output devices during no-signal periods. This design could be portable and operated by batteries if this current is low enough.

- Output stage voltage swing =  $18 V_{p-p} \underline{minimum}$  into a 100  $\Omega$  resistive load. [The more swing, the more power output, and the louder the music can play without clipping distortion, so choose your components wisely!] [Your kit contains a 100  $\Omega$ , 5 %, 5 watt 6.101 load resistor for all measurements on this amplifier.]
- Slew rate: No visible slewing allowable within the frequency range of 5 Hz to 20 kHz at full output into 100  $\Omega$ .

2. Construct the amplifier you have designed and verify its performance by appropriate measurements. <u>WARNING: The metal cans of the output devices are connected to the</u> collector, which is connected to  $V_{CC}$  or  $V_{EE}$ . Be careful not to touch the leads of other parts to

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**these cans!** These should include semilog frequency response [bode-amplitude only] plots to identify the low and high frequency -3dB points, offset voltage measurements, slew rate measurements. You should also measure the output resistance by measuring the open circuit  $v_{out}$  and the loaded  $v_{out}$ ; likewise the input resistance: use a known source resistance high enough to make a voltage divider at the input when it is connected in series with the function generator. Input and output resistance measurements should be made with a 1 kHz sine wave input; frequency response measurements should always be referenced to 1 kHz in audio work, but are often referenced to 400 Hz in radio work.

To measure the input resistance, you could place a pot in series with the input, and then measure the ac signal voltage at the input while you turn the pot up until the input voltage drops from full input [start with the pot turned down =  $\sim$ 0 resistance] to -6dB. At this point the resistance of the pot will equal the input resistance.

[The output impedance is very low, so use the DMM to compare the loaded and unloaded output voltages. The DMM should be used for all measurements where its frequency response permits, as it is much more accurate than the oscilloscope, which is only good for about 5-10% accuracy.]

You will need to load the output with a very small resistance in order to see any change in output voltage between the open circuit [unloaded] and loaded output voltage. Also, to use a low load resistance, you must reduce the input signal to keep the dissipation in the output devices down. You may only be able to accommodate around 1 V RMS at the output before you start to overheat the outputs or the low value load resistance. Anyway, the idea is to measure the open-circuit and closed-circuit output voltages at 1000 Hz, and then you can calculate the source impedance knowing the value of the load resistance. It is a very small number, although it rises at high frequencies as feedback falls off.

- Amplify 1 kHz and 10 kHz triangle waves and notice that very little distortion is evident as compared with the amplifier that you constructed in experiment 5 of Lab 4. **Q 1.7 How can you explain this?**
- Amplify 10 Hz, 1 kHz, and 10 kHz square waves and sketch the output waveforms. **Q 1.8 How do** you explain any differences you see between the input and the output voltages?

Change the feedback connection from the output of the complementary-symmetry power stage to the output of the op-amp. **[Q 1.9 What characteristic of the emitter-follower allows us to do this?]** Repeat the two test series immediately above and note any differences. **Q 1.10 Explain the differences.** 

3. Q 1.11 If the amplifier had been built without the output stage, what happens to the amplifier gain and output swing if the smallest safe value of load resistor that you calculated above were connected directly to the output of the opamp? Q 1.12 What is the function of the output stage of this amplifier? Q 1.13 How does it affect the output impedance of the amplifier?

4. Reconnect the output stage to your amplifier and remove the diode biasing circuitry from the output stage and observe the increase in crossover distortion when the resistor you calculated above loads the amplifier. Note that you will have to connect the output of the opamp directly to the bases of transistors  $Q_1$  and  $Q_2$ . [Tie the bases together.] [When the TA demonstrates your amp with the CD player, repeat this step while listening to music. Keep the signal level low at first to hear the maximum crossover distortion, then turn up the level, and the distortion seems to disappear.

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# [Q 1.14 Why?]

5. Reconnect the amplifier as originally shown in Figure 1. Observe the maximum clean peak-peak output voltage swing into the 100  $\Omega$  load at 1000 Hz. Now connect the output of the op-amp to the junction between diodes D<sub>1</sub> and D<sub>2</sub> instead of to the base of the PNP transistor. What difference does this change make in the output voltage swing? **[Q 1.15 Why?]** 

6. Demonstrate your circuit to the TA. <u>You must sign up for a checkoff in advance. The signup</u> sheet will be posted on the door to 38-601. Your circuit must be working properly before the <u>checkoff time: checkoff is NOT the time to debug your circuit.</u> The TA will question you to determine your understanding of the circuit, ask you to demonstrate some measurements, and will test your circuit with a CD player and loudspeaker. Bring your favorite CD if you wish. <u>KEEP THIS</u> <u>CIRCUIT BUILT ON YOUR NERDKIT, AS YOU WILL NEED IT FOR LAB. NO. 6</u>.

# Experiment 2: Differential Transistor Pair [Long-Tailed Pair]

In this experiment, you will investigate the performance of a differential amplifier input stage and examine its significant characteristics. Please enter your data in the table provided.



Figure 2: Differential amplifier for experiment 2.

[Please note that without the emitter linearizing resistors, this amplifier is operating without any feedback. Keep your eye on the purity of the output signal on your scope and see if there are any differences between the circuits with the emitter resistors and the ones without them. You may have to use a fairly large output swing in order to see any distortion. **Q 2.1 Write comments on this in your lab report.**]

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1. Construct the differential amplifier of Figure 2. Connect a 1 kHz signal to both inputs  $v_{in}^{+}$  and  $v_{in}^{-}$ . Measure the common-mode gain:

$$A_{cm} = v_{out} \div \left(\frac{v_{in}^{+} + v_{in}^{-}}{2}\right)$$

Now measure the "single-ended" differential gain. You can do this by grounding the negative input and applying a signal to the positive input and by appropriately adjusting the result. \*

$$A_{diff} = \frac{v_{out}}{v_{in}} - \frac{A_{cm}}{2}.$$

[\* This adjustment is required because we are not applying a true differential input voltage, but rather simulating one with a single input voltage. This has the effect of also applying an average common-mode input voltage equal to  $\frac{v_{in}^{+} + v_{in}^{-}}{2} = \frac{v_{in}^{+} + 0}{2} = \frac{v_{in}^{+}}{2}$  at the same time, so some of the output is due to common-mode gain, not just differential gain.]

### Q 2.2 How can you tell which input is the positive input?

Finally, measure the output-offset voltage [with no AC input signal] across the differential output terminals [collector-collector rather than second collector to ground]. Make sure the  $12k\Omega$  resistors are exactly equal to avoid generating an offset voltage due to unequal resistor values.

2. Now replace the emitter resistors with short circuits and repeat the measurements in step 1 above.

Table for Differential Amplifier Results						
Circuit	A <sub>cm</sub>	A <sub>diff</sub> Single-ended	Output Offset Voltage	CMRR		
2N3904's						
470 Ω R <sub>E</sub> 's						
15kΩ Tail						
Resistor						
2N3904's						
No R <sub>E</sub> 's						
15kΩ Tail						
Resistor						
LM394						
470 Ω R <sub>E</sub> 's						
15kΩ Tail						
Resistor						
LM394						
No R <sub>E</sub> 's						
15kΩ Tail						
Resistor						

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2N3904's		
470 Ω R <sub>E</sub> 's		
Current source		
2N3904's		
No R <sub>E</sub> 's		
Current source		
LM394		
470 Ω R <sub>E</sub> 's		
Current source		
LM394		
No R <sub>E</sub> 's		
Current source		

3. Next, obtain an LM394 supermatched pair [2 devices on one chip], and repeat steps 1 and 2 above using the new device.



Figure 3: Current source for experiment 2.

- 4. Replace resistor R<sub>x</sub> in your differential amplifier with the current source of Figure 3. Repeat all your measurements in steps 1-3 above using the current source. Since there are no AC input resistance considerations, we can choose R<sub>B</sub> to be very low for the current source, to make sure that transistor Beta does not affect the value of the current through the current source. IMPORTANT: Design your current source to give exactly the same total current as that which flowed through the resistor R<sub>x</sub> in the previous circuit. [Use very stiff voltage divider biasing, i.e. make the current through R<sub>1</sub> and R<sub>2</sub> very large compared to the transistor base current.
- 5. Calculate the common-mode rejection ratios for all circuit configurations. Express your results in dB. Tabulate all your data from steps 1-5 in the table provided so that the various circuits can be

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easily compared. Q 2.3 Make some remarks in your write up about which configurations and devices are the best with respect to CMRR, voltage gain, and low offset voltage.

$$cmrr = \left| \frac{A_{_{diff}}}{A_{_{cm}}} \right|$$

6. Here are some equations for the differential amp that you can use to compare with your measurements:

$$I_{x} = I_{E_{1}} + I_{E_{2}}$$

$$v_{IN}^{+} - v_{be1} - v_{be2} - v_{IN}^{-} = 0$$
or  $v_{be1} - v_{be2} = v_{IN}^{+} - v_{IN}^{-}$ 

$$\begin{split} A_{cm} &= v_{out} \div \left(\frac{v_{in}^{+} + v_{in}^{-}}{2}\right) = \frac{-g_m R_L}{1 + g_m \left(2R_x + R_E\right) \left(1 + \frac{1}{\beta_o}\right)} = \frac{-\beta_o R_L}{r_\pi + \left(2R_x + R_E\right) \left(\beta_o + 1\right)} \approx \frac{-R_L}{2R_x + R_E} \\ A_{diff} &= \frac{v_{out}}{v_{indiff}} = \left(\frac{1}{2}\right) \left(\frac{-R_L}{R_E}\right); \ or &= \frac{-g_m R_L}{2} = \frac{-\beta_0 R_L}{2r_\pi} \ if \ R_E = 0. \end{split}$$

#### Experiment 3: 555 Timer Chip

In this experiment you will investigate the performance of the 555-timer chip that you will find in your laboratory kit. You will have to refer to the 555 data sheet that was handed out in class. This data sheet shows both the schematic for the 555 and some typical applications.



Figure by MIT Opencourseware.

Figure 4: Astable Oscillator using 555 Timer Chip

1. Construct an astable oscillator, operating from the +15 V supply in your lab kit, which produces an output of 10 kHz with a duty cycle in excess of 0.1. Note that to avoid damaging your 555, you should

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not use resistor values less than 1 k $\Omega$  in the timing portion of your circuit. With the frequency of your oscillator set to 10 kHz, measure the duty cycle. <u>Note: The 555, along with some other timer</u> chips, generates a very big [ $\approx 150 mA$ ] supply-current glitch during each output transition. Be sure to use a hefty (= 100  $\mu$ F) bypass capacitor from the chip V <sub>cc</sub> pin to ground, physically near the chip. Even so, the 555 may have a tendency to generate double output transitions. Most of the CMOS versions of the 555 do not have this problem and also draw far less current, can swing rail-to-rail at the output, and can operate down to 1 or 2 volts V<sub>cc</sub>!

2. Without changing any of the component values in your circuit, reconnect **all of** your circuit to operate from the +5 V supply in your lab kit. Measure the frequency and the duty cycle and compare with the values you found in part 1. **Q 3.1 Why do these values vary so little with supply voltage?** 

3. You can use the 555 chip to generate a sawtooth waveform, instead of the square wave available from output pin 3. One way to do this is to drive the capacitor with a current source (which will give a linear capacitor voltage with time) and to reset the capacitor (discharge it) with the 555 discharge connection. Design and construct such a circuit to generate a 10kHz sawtooth waveform with a reset time less than 1 % of the period of the sawtooth. Construct your current source using the 2N5459 FET in the configuration shown in Figure 5. The FET characteristics and the value of the resistor R determine the current supplied by this source. Note: to protect your 555 from damage when discharge path. However, this resistor will distort the sawtooth waveform if it is located as shown above [ $R_B$ ]. You may relocate this resistor so that it is still in series with pin 7, but not in the charging path. You may also eliminate this resistor entirely if your timing capacitor is small enough so that the transistor saturation resistance will limit the discharge current to safe levels.



Figure 5: JFET current source.

4. Using the 555 timer IC, design and construct a voltage-controlled sawtooth oscillator. Your design objective should be a frequency variation of about 100 Hz to 10 kHz as the input voltage is varied from <u>approximately</u> 0 to 15 volts. You may use a pot to provide the adjustable control voltage. You can use the DC offset voltage from your function generator as a control voltage. One of the circuits you should consider is the "voltage controlled current source" [VCCS] on the next page. The output transistor of this circuit connects in place of resistor R<sub>A</sub>. You may find that this circuit works better with your 555 if you connect [only] the 555 between ground [to the 555 V<sub>CC</sub> terminal] and –15 volts [to the 555 ground terminal].

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Your write-up should show your design and also list the lowest and highest frequencies that you obtained from your design.

# VOLTAGE-CONTROLLED CURRENT SOURCE [VCCS]



- 1. Feedback forces  $[+15V V_{IN}]$  across R<sub>E</sub>, because V<sub>+</sub> must equal V<sub>-</sub>
- 2. If we ignore any offset voltage at the output of the op-amp, the only error comes from the emitter current not quite being equal to the collector current [due to  $I_B$ ]. One can use a Darlington transistor or a JFET to reduce or remove this error.
- 3. This version of the VCCS does not work if  $V_{IN}$  is an external voltage not referenced to  $V_{CC}$ .
- 4. Example:  $R_E = 100\Omega$ ,  $\beta_F = 100$ ,  $V_{IN} = 5$  V, 10 V, and 14 V:

 $[15V-5V] / 100\Omega = 100 \text{ mA for } I_E; I_C = 99 \text{ mA}.$ 

 $[15V-10V] / 100\Omega = 50 \text{ mA for } I_E; I_C = 49.5 \text{ mA}.$ 

 $[15V-14V] / 100\Omega = 10 \text{ mA for } I_E; I_C = 9.9 \text{ mA}.$ 

5.  $R_1 - R_2$  can of course be a potentiometer for ease of adjustment!

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Cite as: Ron Roscoe, course materials for 6.101 Introductory Analog Electronics Laboratory, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/), Massachusetts Institute of Technology. Downloaded on [DD Month YYYY].