MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.374: Analysis and Design of Digital Integrated Circuits
Problem Set # 1 Solutions

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Problem 1: Device Parameters

The data from five measurements made on a short channel NMOS device appears in Table 1. Given that $V_{DSAT} = 0.6\ V$ and $k' = 100\ \mu A/V^2$, calculate V_{T0}, γ, λ, $2|\phi_F|$, and W/L.

Table 1: Measured Data for Short Channel NMOS

Meas. Number	V_{GS}	V_{DS}	V_{BS}	$I_D(\mu A)$
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	-1	1146
5	2	1.8	-2	1039

Solution

Using the data from the table, set up equations containing the unknowns of interest. We will use the unified MOSFET model for our analysis: $k_n'W/L(V_{GT}V_{min} - V_{min}^2/2)(1+\lambda V_{DS}) = I_o$.

Let us first make an assumption about the region of operation. The minimum V_{GS} is 2, and we can guess that V_{to} is less than half a volt, so $V_{GT} > V_{DSAT}$. Additionally, the minimum V_{DS} is greater than V_{DSAT}. Unless V_{to} is abnormally high, the device is in the velocity saturation region for all the data points. We can check this assumption at the end of the problem. Using this assumption, the first three data points give us the following equations

$$100 \cdot \frac{W}{L} \cdot \left((2.5 - V_{to}) \cdot 0.6 - \frac{0.6^2}{2}\right) \cdot (1 + \lambda \cdot 1.8) = 1812\mu$$

$$100 \cdot \frac{W}{L} \cdot \left((2 - V_{to}) \cdot 0.6 - \frac{0.6^2}{2}\right) \cdot (1 + \lambda \cdot 1.8) = 1297\mu$$

$$100 \cdot \frac{W}{L} \cdot \left((2 - V_{to}) \cdot 0.6 - \frac{0.6^2}{2}\right) \cdot (1 + \lambda \cdot 2.5) = 1361\mu$$

These are three equations with three unknowns - piece of cake! Divide the first two equations to get:

$$\frac{\left((2.5 - V_{to}) \cdot 0.6 - \frac{0.6^2}{2}\right)}{\left((2 - V_{to}) \cdot 0.6 - \frac{0.6^2}{2}\right)} = \frac{1812}{1297}.$$ Simplifying gives: $1.5 - 0.6V_{to} - 0.18 = 1.397 \cdot (1.2 - 0.6V_{to} - 0.\dot{1}8)$

and $0.2382V_{to} = 0.1049$ and $\boldsymbol{V_{to} = 0.44\ V}$.

Dividing the second and third equations gives:

$\frac{(1+\lambda\cdot 1.8)}{(1+\lambda\cdot 2.5)} = \frac{1297}{1361}$. Solving for λ gives λ = **0.08**

Plugging these two parameters into the first equation gives: $\frac{W}{L}$ = **15**.

Writing two equations from the last two data points permits us to solve for the remaining two unknowns:

$1716\cdot((2-V_{T1})\cdot 0.6-0.18) = 1146$ so $V_{T1} = 0.5869$.

$1716\cdot((2-V_{T2})\cdot 0.6-0.18) = 1039$ so $V_{T2} = 0.6909$.

Now we use the equation for threshold voltage to relate the remaining unknowns:

$0.44+\gamma\cdot(\sqrt{2\phi_F+1}-\sqrt{|2\phi_F|}) = 0.5869$

$0.44+\gamma\cdot(\sqrt{2\phi_F+2}-\sqrt{|2\phi_F|}) = 0.6909$

Subtracting 0.44 from both sides and dividing the equations gives:

$\frac{(\sqrt{2\phi_F+2}-\sqrt{|2\phi_F|})}{(\sqrt{2\phi_F+1}-\sqrt{|2\phi_F|})} = 1.7$. Simplifying gives: $1.7\cdot\sqrt{|2\phi_F|+1} = \sqrt{|2\phi_F|+2}+0.7\cdot\sqrt{|2\phi_F|}$.

Squaring both sides gives: $2.89\cdot(|2\phi_F|+1) = |2\phi_F|+2+0.49\cdot|2\phi_F|+1.4\cdot\sqrt{|2\phi_F|}\cdot\sqrt{|2\phi_F|+2}$.

Collecting terms gives: $1.4\cdot|2\phi_F|+0.89 = 1.4\cdot\sqrt{|2\phi_F|^2+2\cdot|2\phi_F|}$. Squaring both sides and solving gives: $|2\phi_F|$ = **0.556**.

We can plug this value back into either threshold voltage equation to get γ = **0.293**.

Problem 2: Backgate Effect

The circuit in Fig. 1 is known as the *source follower* configuration. It achieves a DC level shift between the input and the output. The value of this shift is determined by the current I_0. Assume x_d=0, γ=0.4, $2|\phi_f|$=0.6V, V_{T0}=0.43V, k_n'=115μA/V^2 and λ=0.

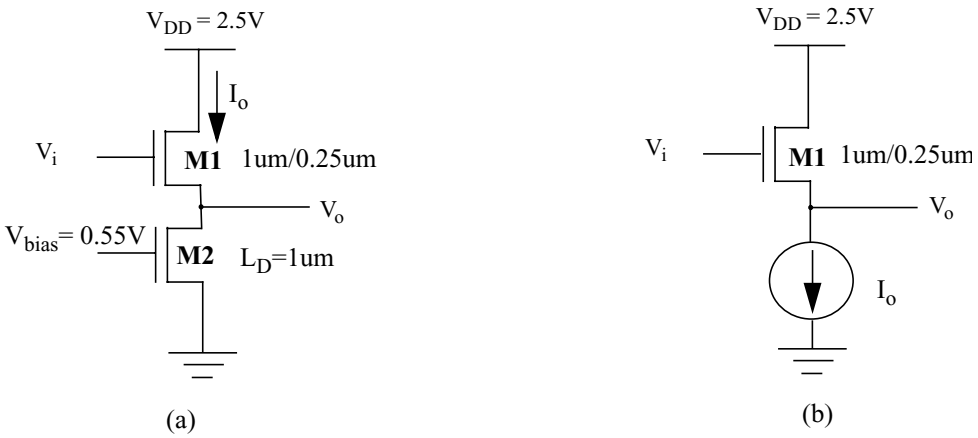


Figure 1: NMOS source follower configuration

a) Suppose we want the nominal level shift between V_i and V_o to be 0.6V in the circuit in Figure 1(a).

Neglecting the backgate effect, calculate the width of M2 to provide this level shift (Hint: first relate V_i to V_o in terms of I_o).

Solution

The level shift of 0.6 tells us that V_{GS1}=0.6 so V_{GT1}=0.17. This means that **M1** must be in the saturation region (not velocity saturated). Thus,

$\frac{k'_n \cdot \frac{W}{L}}{2} \cdot (V_{GS} - V_T)^2 = I_D$, and I_D=6.647μ A.

For **M2**, V_{GT}=0.12, so **M2** also is in the saturation region (not velocity saturated). Using the same equation as above and solving for W/L gives **W/L = 8.**

b) Now assume that an ideal current source replaces M2 (Figure 1(b)). The NMOS transistor M1 experiences a shift in V_T due to the backgate effect. Find V_T as a function of V_o for V_o ranging from 0 to 2.5V with 0.5V intervals. Plot V_T vs. V_o.

Solution

The threshold voltage equation provides the relation that we need:

$$V_T = V_{T0} + \gamma \cdot (\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}) = V_{T0} + \gamma \cdot (\sqrt{|2\phi_F| + V_o} - \sqrt{|2\phi_F|}).$$

See the graph at the end of this problem.

c) Plot V_o vs. V_i as V_o varies from 0 to 2.5V with 0.5 V intervals. Plot two curves: one neglecting the backgate effect and one accounting for it. How does the backgate effect influence the operation of the level converter?

At V_o(with backgate effect) = 2.5V, find V_o(ideal) and thus determine the maximum error introduced by the backgate effect.

Solution

To plot V_o versus V_i, we need to relate V_o to V_i. We can do this by solving the current equation (**M1** should remain in the same region to first order because V_{GT} will remain roughly constant to maintain the correct drain current) for V_i:

$$V_i = V_o + V_T + \sqrt{\frac{2I_D}{k'_n \cdot \frac{W}{L}}}$$

The maximum error occurs at the highest V_{SB}. At Vo = 2.5, the error is 3.4944-3.1=**0.3944** V.

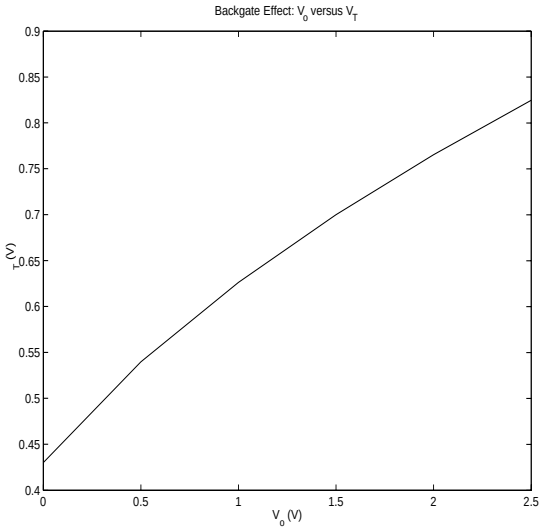


Figure for Problem 2(b)

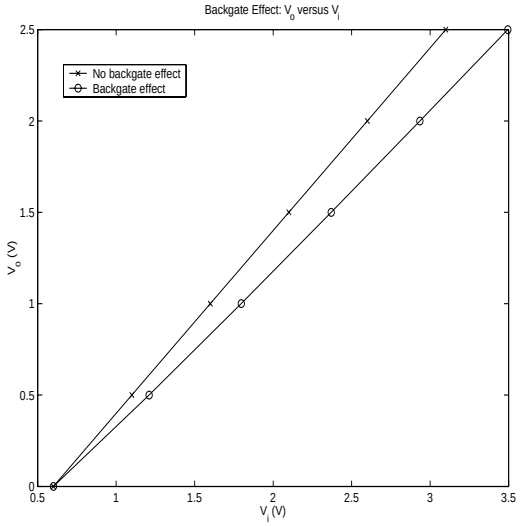


Figure for Problem 2(c)

Problem 3: Velocity Saturation

This problem explores the behavior of short-channel devices. For the HSPICE simulations of this problem you will use the 0.18u model parameters. Use the **HSPICE model parameters** which can be found in " log018_1.l "

a) Using HSPICE plot I_D versus V_{DS}, for the transistor of the following figure, with V_{GS} (0.6V, 0.8V, 1V, 1.2V, 1.4V, 1.6V, 1.8V) as a parameter. Comment on the dependence of I_D with respect to V_{GS}.

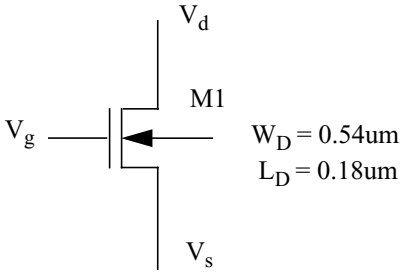
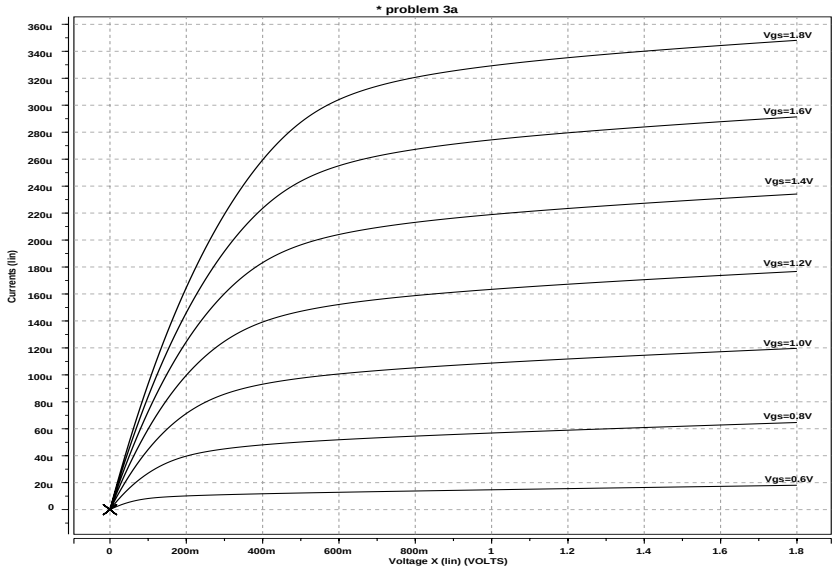


Figure 2: Short channel Transistor.

Solution

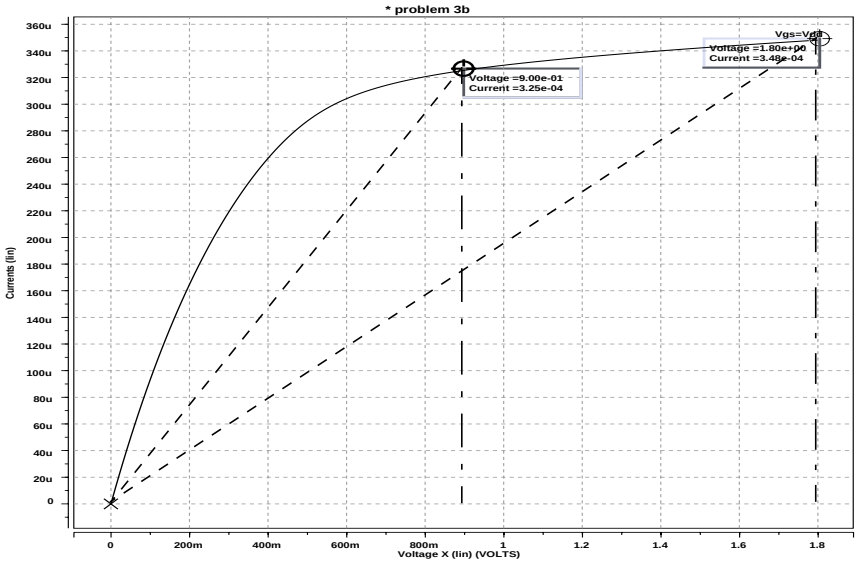
The I_D plots are shown in the next graph.



It is clear from the curves that, for the short channel device, there is a linear dependence of the saturation current with respect to V_{GS}.

b) Calculate the effective resistance for a high to low transition, using the method described in slide 44 (Handout 2).

Solution



We can use the following expression:

$$R_{eff} = \frac{1}{2}\left(\left(\frac{V_{DS}}{I_D}\right)_{V_{DS}=V_{DD}} + \left(\frac{V_{DS}}{I_D}\right)_{V_{DS}=V_{DD}/2}\right)$$

We can find the values of the drain current from the plot. So

$$R_{eff} = \frac{1}{2}\left(\frac{1.8}{0.3481 \cdot 10^{-3}} + \frac{0.9}{0.3254 \cdot 10^{-3}}\right) = 4K\Omega$$

c) Consider two CMOS inverters with $(W_1/L_1)_n$=(2.88u/1.44u), $(W_1/L_1)_p$=(5.76u/1.44u) and $(W_2/L_2)_n$=(0.36u/0.18u), $(W_2/L_2)_p$=(0.72u/0.18u). Assume V_{DD} = 1.8 V and the output of the inverter is loaded by C_L=100fF capacitance. Calculate the propagation delay t_P and check the answers with HSPICE.

Solution

The propagation delay t_p is the average of t_{pHL} and t_{pLH}. We can use the next equations to calculate the rise and fall times for the two inverters.

$$t_{pHL} = 0.69R_{eqHL}C_L \text{ and } t_{pLH} = 0.69R_{eqLH}C_L$$

Inverter 1

for a high to low transition (we assume that the PMOS is off):

$$R(V_{DS} = 1.8V) = 1.8V/0.339m = 5.3K\Omega \text{ and } R(V_{DS} = 0.9V) = 0.9V/0.319m = 2.8K\Omega$$

$$R_{eq} = \frac{1}{2}(5.3K + 2.8K) = 4.05K\Omega$$

$$t_{pHL} = 0.69(4.05K)(100f) = 0.28ns$$

for a low to high transition (we assume that the NMOS is off):

$$R(V_{DS} = -1.8) = -1.8V/-0.162m = 11.1K\Omega \text{ and } R(V_{DS} = -0.9V) = -0.9V/-0.150m = 6.0K\Omega$$

$$R_{eq} = \frac{1}{2}(10.5K + 5.7K) = 8.6K\Omega$$

$$t_{pLH} = 0.69(8.1K)(100f) = 0.59ns$$

So, $t_{p1} = \frac{1}{2}(t_{pHL} + t_{pLH}) = 0.435ns$

Inverter 2

for a high to low transition (we assume that the PMOS is off):

$$R(V_{DS} = 1.8V) = 1.8V/0.254m = 7.1K\Omega \text{ and } R(V_{DS} = 0.9V) = (0.9V)/0.237m = 3.8K\Omega$$

$$R_{eq} = \frac{1}{2}(7.1K + 3.8K) = 5.45K\Omega$$

$$t_{pHL} = 0.69(5.45K)(100f) = 0.38ns$$

for a low to high transition (we assume that the NMOS is off):

$$R(V_{DS} = -1.8V) = -1.8/-0.172m = 10.5K\Omega \text{ and } R(V_{DS} = -0.9V) = -0.9/-0.147m = 6.4K\Omega$$

$$R_{eq} = \frac{1}{2}(6.4K + 10.5K) = 8.5K\Omega$$

$$t_{pLH} = 0.69(7.9K\Omega)(100f) = 0.58ns$$

So, $t_{p2} = \frac{1}{2}(t_{pHL} + t_{pLH}) = 0.48ns$

The HSPICE simulation gives for the propagation delay:

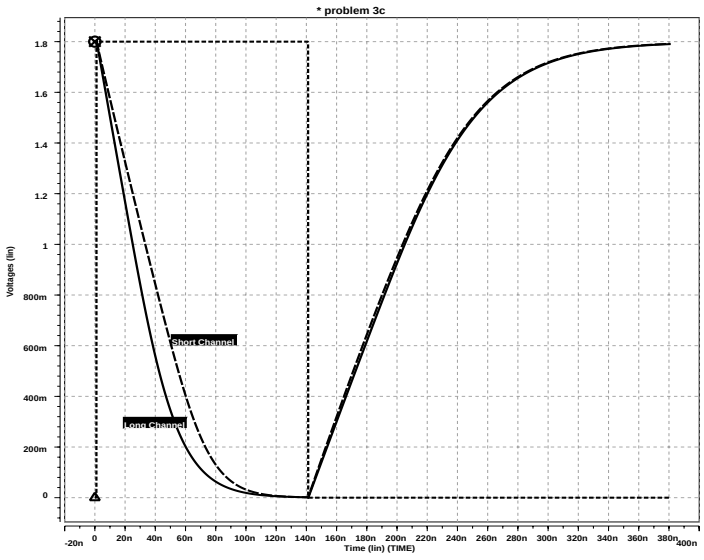
$$t_{p1} = \frac{0.45n + 0.8n}{2} = 0.625ns \text{ and } t_{p2} = \frac{0.39 + 0.59n}{2} = 0.49ns$$

Comment.

Hspice simulations give different results than the hand calculations, because there are some second order effects that affect the performance of the devices. If you perform a transient analysis, you will see that in the case of the long channel inverter, there is an overshoot(undershoot) when the new input data arrives. That's because of clock feedthrough (gate-to-drain capacitive coupling - Chapter 6). The long channel inverter experiences this more intensively, because of the larger sizes of the transistors.

If you make the output load capacitance fairly large then this effect won't be so obvious, and the inverter with the long channel devices will be faster as expected.

This is shown in the next figure.



The difference for the two transitions, comes from the fact that the for the low-to-high transition the currents forthe two inverters are almost the same..

d) Repeat part c) sweeping the supply voltage V_{DD} from 0.4V to 1.8V (sweep step 0.2V). Plot the propa-

gation delay $t_P$versus the supply voltage V_{DD} in the same graph. Comment on the results.

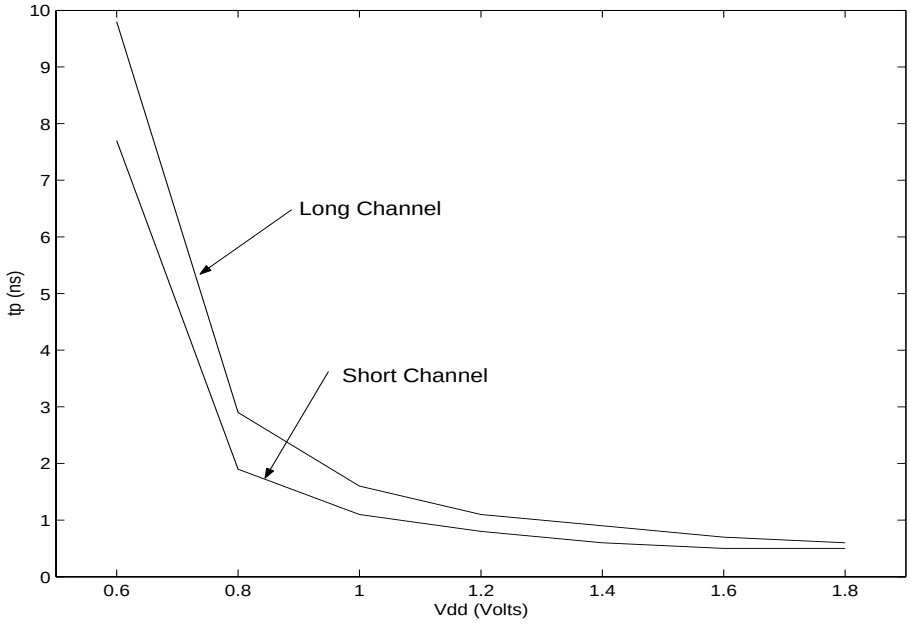
Solution

The next table summarizes the propagation delays for the different supply voltages

V_{DD} (V)	t_{Pinv1} (ns)	t_{Pinv2} (ns)
0.4	X	X
0.6	9.8	7.7
0.8	2.9	1.9
1	1.6	1.1
1.2	1.1	0.8
1.4	0.9	0.6
1.6	0.7	0.5
1.8	0.6	0.5

Table 2: Propagation Delays for the two inverters

The plot is shown in the next figure.



Comments

We see that the curve for the short channel device flattens (~1.4 V), since I_D is linear with respect to V_{GS}.

Problem 4: Voltage transfer characteristics, Noise Margins

The next figure shows an all NMOS inverter.

a) Calculate V_{OH}, V_{OL}, V_M for the inverter.

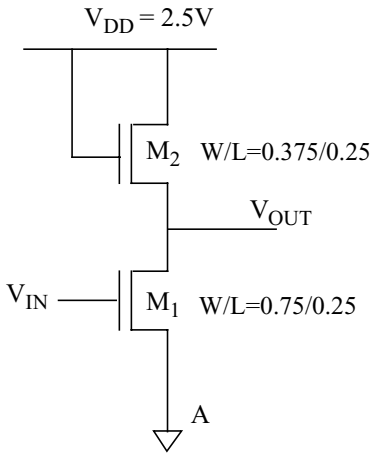


Figure 3: Two Inverter Implementations

Solution:

V_{OH}: We calculate V_{OH}, when M1 is off. The threshold for M2 is:

$$V_T = V_{T0} + \gamma \cdot (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}),\ V_{SB} = V_{OUT},\ |-2\phi_F| = 0.6V$$

and M2 will be off when: $V_{GS} - V_T = V_{DD} - V_{OUT} - V_T = 0$,

Substitute V_T in the last equation and solve for V_{OUT}.

$$V_{DD} - V_{OUT} - V_T = 2.5 - V_{OUT} - (0.43 + 0.4 \cdot (\sqrt{|0.6 + V_{OUT}|} - \sqrt{|0.6|})) = 0$$

We get **V_{OUT}=V_{OH}=1.765V**

V_{OL}: To calculate V_{OL}, we set V_{IN}=V_{DD}=2.5V.

We expect V_{OUT} to be low, so we can make the assumption that M2 will be velocity saturated and M1 will be in the linear region.

For M2: $I_{D2} = k'_n \cdot \frac{W_2}{L_2} \cdot \left((V_{GS} - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda V_{DS})$ and

for M1: $I_{D1} = k'_n \cdot \frac{W_1}{L_1} \cdot \left((V_{GS} - V_{T0}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right)$

Setting $I_{D1} = I_{D2}$, we get an equation and we solve for V_{OUT}.

We get: **V_{OUT}=V_{OL}=0.263V**, so our assumption holds. We have input 2.5 V instead of V_{OH}, an assumption that is often used. If we instead put V_{OH} at the input, V_{OL}=0.38 V and full credit was given for either solution.

V_M: To calculate V_M we set V_M=V_{IN}=V_{OUT}.

Assuming that both transistors are velocity saturated, then we have the next pair of equations:

$$I_{D1} = k'_n \cdot \frac{W_1}{L_1} \cdot \left((V_M - V_{T0}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda V_M) \text{ and}$$

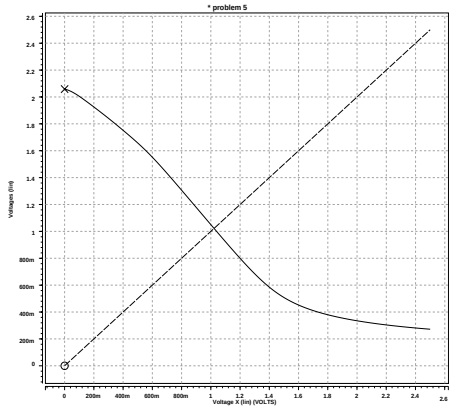
$$I_{D2} = k'_n \cdot \frac{W_2}{L_2} \cdot \left((V_{DD} - V_M - V_T) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right) \cdot (1 + \lambda (V_{DD} - V_M))$$

Setting $I_{D1} = I_{D2}$, we get for **V_M = 1.01 V**

b) Use HSPICE to obtain the VTC.

Solution

The VTC is shown below.



c) Calculate V_{IH}, V_{IL}, and the noise margin and comment on the results. How can you increase the noise margins and reduce the undefined region?

Solution

Circuit 1

V_{IL} = 0.5V, V_{IH} = 1.35V

$NM_H = V_{OH} - V_{IH}$ = 1.765 - 1.35 = 0.42V, $NM_L = V_{IL} - V_{OL}$ = 0.5- 0.26 = 0.24V

We can increase the noise margins by moving V_M closer to the middle of the output voltage swing. Some of you pointed out that the VOH/VOL obtained from HSPICE does not match the value in the hand calculation. This is because, due to diode and leakage currents, the output actually rises higher than VT in order to reach DC steady state and match all the tiny leakage currents. (These are second order effects not modeled by the assumption that Vout should rise to VDD-VT).

d) Comment on the differences in the VTCs, robustness and regeneration between this inverter and a stan-

dard CMOS inverter.

Solution

It is clear from the two VTCs, that a CMOS inverter is more robust, since the low and high noise margins are higher than the first inverter. Also the regeneration in the second inverter is greater since it provides rail to rail output and the gain of the inverter is much greater.

Problem 5: Inverter Gain and Regions of Operation

Figure 0.1 shows a piecewise linear approximation for the VTC. The transition region is approximated by a straight line with a slope equal to the inverter gain at V_M. The intersection of this line with the V_{OH} and the V_{OL} lines defines V_{IH} and V_{IL}.

a) The noise margins of a CMOS inverter are highly dependent on the sizing ratio, r=kp/kn, of the NMOS and PMOS transistors. What ratio 'r' would be required to achieve equal noise margins if the thresholds of NMOS and PMOS were equal and channel length modulation were ignored? Now use HSPICE and the 0.25u process file to test your theory. For your simulation, use Wn=1.0 umso that Wp will just be equal to r*(NMOS mobility/PMOS mobility). If there is a discrepancy in the two results you obtain, suggest some possible explanations.

Solution

The TSMC 0.25µm models were used for simulation and the threshold voltages of NMOS and PMOS devices are nearly equal in this process. A value near r=1 should result in equal noise margins, since the transistors will be closely matched. HSPICE showed that the resulting noise margins for this sizing were N_{MH}=0.97 V and N_{ML}=1.1 V. The mismatch is due to the fact that the PMOS threshold voltage is actually slightly lower, so the PMOS is stronger and the upper noise margin is reduced. In addition, the NMOS velocity saturates at a lower voltage, further increasing the relative strengh of the PMOS when both devices are in velocity saturation. The actual value that results in equal noise margins is r=0.83.

b) Section 5.3.2 of the text uses this piecewise linear approximation to derive simplified expressions for NM_H and NM_L in terms of the inverter gain. The derivation of the gain is based on the assumption that both the NMOS and the PMOS devices are velocity saturated at V_M. For what range of r is this assumption valid? What is the resulting range of V_M?

Solution

Using the equations for finding the region of operation, it can be shown that the PMOS and NMOS are both velocity saturated only while the switching threshold is between 1.06 V and 1.10 V. Since this range may be considered inclusive, we can assume that both devices are velocity saturated and set the currents equal with $V_{IN}=V_{OUT}=V_M$ to find k_p/k_n. Depending on the assumptions we make when we find r, there are a range of possible results. Some people used the definition of r that includes variation in VDSAT for NMOS and PMOS, some included the effect of channel length modulation, and other combinations of the above considerations. Since the problem was slightly ambiguous on this topic full credit will be given for any of the answers.

The equation below gives kp/kn in terms of known circuit parameters. Leaving out channel-length modulation results in slightly different numbers. Then, whether r is defined as kp/kn or (kp*vdsatp)/(kn*vdsatn) produces two different results due to the different definitions.

$$\frac{k_p}{k_n} = \frac{v_{dsatn}\left[v_m - v_{tn} - \frac{v_{dsatn}}{2}\right][1 + \lambda v_m]}{v_{dsatp}\left[v_m - v_{dd} - v_{tp} - \frac{v_{dsatp}}{2}\right][1 + \lambda(v_m - v_{dd})]}$$

TABLE OF 'r' RANGES	VDSAT Included	VDSAT Not Included
Lambda Included	0.54-0.65	0.34-0.41
Lambda Not Included	0.58-0.71	0.37-0.45

Some of you, however, used the equation for r given on page 186, equation 5.6 of the text. Although you coincidentally got the same numbers as one of the results above, this method isn't valid because this equation is for the case when both NMOS and PMOS are saturated, NOT velocity saturated.

This result can be checked by sizing the devices accordingly and testing the resulting V_M in HSPICE. The result gives a range of 1.04 V to 1.09 V. This makes sense, because the NMOS must be much stronger than the PMOS to achieve a switching threshold near 1 V.

c) Derive expressions for the inverter gain at V_M for the cases when the sizing ratio is just above and just below the limits of the range where both devices are velocity saturated. What are the operating regions of the NMOS and the PMOS for each case? Consider the effect of channel-length modulation by using the following expression for the small-signal resistance in the saturation region: $r_{o,sat} = 1/(\lambda I_D)$.

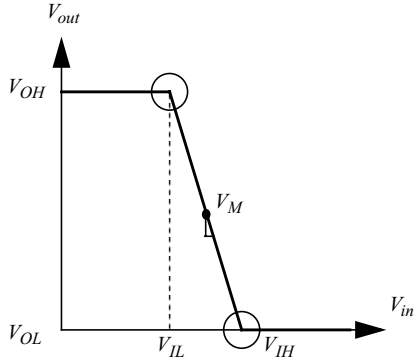


Figure 0.1 A different approach to derive V_{IL} and V_{IH}.

Solution

When V' is slightly smaller than 1.06 V, the PMOS is velocity saturated and the NMOS is saturated. Section 5.3.2 of the text shows this derivation for the case when both devices are velocity saturated. These derivations can be completed by substituting the correct current equations and using the same method. The results are as follows:

For the case when the NMOS is saturated and the PMOS is velocity saturated:

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n(V_{in} - V_{tn})(1 + \lambda_n V_{out}) + k_p V_{DSATP}(1 + \lambda_p(V_{out} - V_{DD}))}{\frac{k_n\lambda_n}{2}(V_{in} - V_{tn})^2 + k_p V_{DSATP}\lambda_p\left(V_{in} - V_{DD} - V_{tp} - \frac{V_{DSATP}}{2}\right)}$$

Dropping the second order terms in the numerator, substituting V_m for V_{in}, and simplifying the denominator leads to the following expression for the gain:

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n(V_m - V_{tn}) + k_p V_{DSATP}}{I_D(V_m)(\lambda_n - \lambda_p)}$$

Problem 6: Static CMOS Inverter

For this problem use scalable CMOS design rules and assume:

V_{DD} = 2.5V, W_P/L = 1.25/0.25, W_N/L = 0.375/0.25, $L=L_{eff}$ =0.25µm (i.e. x_d= 0µm), $C_L=C_{inv\text{-}gate}$, k_n' = 115µA/V^2, k_p'= -30µA/V^2, V_{tn0} = | V_{tp0} | = 0.4V, λ = 0V^{-1}, γ = 0.4, 2|ϕ_f|=0.6V, and t_{ox} = 58A. Use the Hspice model parameters for parasitic capacitance given below (i.e. C_{gd0}, C_j, C_{jsw}), and assume that V_{SB}=0V for all problems except part **(e)**.

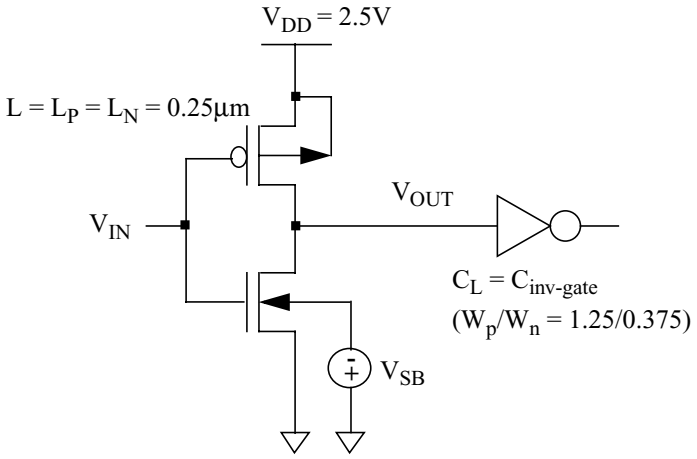


Figure 4: CMOS inverter with capacitive load.

Parasitic Capacitance Parameters (F/m)##
NMOS
CGDO=3.11x10^{-10}, CGSO=3.11x10^{-10}, CJ=2.02x10^{-3}, CJSW=2.75x10^{-10}

PMOS
CGDO=2.68x10^{-10}, CGSO=2.68x10^{-10}, CJ=1.93x10^{-3}, CJSW=2.23x10^{-10}

a) What is the V_m for this inverter?

Solution

Assume that Vm is around midrail (1.25V). That means that the NMOS is velocity saturated and the PMOS is saturated. To find Vm, we set the sum of the currents at Vout equal to 0 using the correct equation for each device:

$k_n \cdot V_{DSATn} \cdot \left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p \cdot 0.5 \cdot (V_M - V_{DD} - V_{Tp})^2 = 0$. Plug in numbers:

$$172.5 \cdot 0.6 \cdot (V_M - 0.4 - 0.315) + (-150) \cdot 0.5 \cdot (V_M - 2.5 - (-0.4))^2 = 0$$

$$103.5 V_M - 74 - (-75 \cdot (V_M{}^2 - 4.2 V_M + 4.41)) = 0.$$

Solving this quadratic gives $\boldsymbol{V_M = 1.245\,V}$.

b) What is the effective load capacitance C_{Leff} of this inverter? (include parasitic capacitance, refer to notes for K_{eq} and m.) **Hint:** You must assume certain values for the source/drain areas and perimeters since there is no layout. For our scalable CMOS process, λ = 0.125 μm, and the source/drain extensions are 5λ for the PMOS; for the NMOS the source/drain contact regions are 5λx5λ.

Solution

The calculation of the lumped load capacitance follows the format presented in the lecture notes. The only difference is the dimensions of the devices.

$C_{Leff} = C_L + C_{parasitic} = C_{g3} + C_{g4} + C_{db1} + C_{db2} + C_{gd1} + C_{gd2}$.

$\mathbf{C_{g3}} = (C_{GD0n} + C_{GSOn})W_n + C_{ox}W_nL = 2(3.11e\text{-}10)(0.375e\text{-}6) + 6e\text{-}15(0.375)(0.25) = \mathbf{0.796fF}$

$\mathbf{C_{g4}} = (C_{GD0p} + C_{GSOp})W_p + C_{ox}W_pL = 2(2.68e\text{-}10)(1.25e\text{-}6) + 6e\text{-}15(1.25)(0.25) = \mathbf{2.545fF}$

$\mathbf{C_{db1}} = K_{eqn}(AD_n)C_j + K_{eqswn}(PD_n)C_{jsw}$. Need to do this calculation for both transitions and average the results. The Keq values are already calculated in the notes.

$AD_p=AS_p=1.25um*0.625um=0.78125um^2$ and $AD_n=AS_n=0.125*0.375+0.625^2=0.4375um^2$.

$PD_p=PS_p=2*0.625um+1.25um=2.5um$ and $PD_n=PS_n=5*0.125um*3+(2+1+1)*0.125um=2.375um$.

(0.57*0.4375*2 + 0.61*2.375*0.28) = 0.904fF for HL transition

(0.79*0.4375*2 + 0.81*2.375*0.28) = 1.23fF for LH. Average $\mathbf{C_{db1}=1.067fF}$.

$\mathbf{C_{db2}} = K_{eqp}(AD_p)C_j + K_{eqswp}(PD_p)C_{jsw}$.

(0.79*0.78125*1.9 + 0.86*2.5*0.22) = 1.65fF for HL transition

(0.59*0.78125*1.9 + 0.7*2.5*0.22) = 1.26fF for LH. Average $\mathbf{C_{db2}=1.455fF}$.

$\mathbf{C_{gd1}} = 2C_{GD0n}W_n = 2*3.11e\text{-}10*0.375e\text{-}6 = \mathbf{0.233fF}$.

$\mathbf{C_{gd2}} = 2C_{GD0p}W_p = 2*2.68e\text{-}10*1.25e\text{-}6 = \mathbf{0.67fF}$.

$\mathbf{C_L}$ = sum = **6.767fF**. Note - since the problem states that x_d=0, it is ok if you neglected the last two parasitic capacitances. We intended for them to be included, though.

c) Calculate t_{PHL}, t_{PLH} assuming the result of (b) is 'C_{Leff} = 6.5fF'. (Assume ideal step input, i.e. t_{rise}=t_{fall}=0. Do this part by computing the average current used to charge/discharge C_{Leff}.)

Solution

We can estimate the propagation delay using the approximation $\Delta t = \Delta Q/I$, where $\Delta Q = C_{Leff}V_{DD}$ and I is

the average current used to charge/discharge C_{Leff}. During the high-to-low transition C_{Leff} is discharged through the NMOS transistor so $I = I_{avgN}$. During the low-to-high transition C_{Leff} is charged through the PMOS transistor so $I = I_{avgP}$. In summary

$$t_{delay} \cong \frac{V_{DD} \cdot C_{Leff}}{2 \cdot I_{avg}}, \text{ where } I_{avgN} = \frac{I_{ds}(V_o = 0) + I_{ds}\left(V_o = \frac{V_{DD}}{2}\right)}{2}, I_{avgP} = \frac{I_{ds}(V_o = V_{DD}) + I_{ds}\left(V_o = \frac{V_{DD}}{2}\right)}{2}$$

Table 3 shows corresponding values for I_{avgN}, I_{avgP}, t_{PLH}, and t_{PHL}. NOTE- This solution included channel

	V_o (V)	Operation Mode	I_{ds} (mA)	I_{avg} (mA)	Prop Delay (ps)
for t_{PLH}	0	PMOS vel sat.	0.300	0.285	28.5
	1.25	PMOS vel sat	0.270		
for t_{PHL}	2.5	NMOS vel sat.	0.209	0.202	40.0
	1.25	NMOS vel sat	0.195		

Table 3: Average currents and propagation delays for Problem 4(c).

length modulation, but it is ok if your solution did not (see problem assumptions).

d) Find (W_p/W_n) such that $t_{PHL} = t_{PLH}$.

Solution

One way to do this is to solve the current average equations for W_p/W_n after setting the propagation delays equal to one another. A much easier method is to sweep the widths in HSPICE. The HSPICE sim shows that **W_p/W_n =2.6** gives equal rise and fall times.

e) Suppose we increase the width of the transistors to reduce the t_{PHL}, t_{PLH}. Do we get a proportional decrease in the delay times? Justify your answer.

Solution

The propagation delays DO NOT decrease in proportion to the widths because of self-loading effects. As the device size increases, its parasitic capacitances increase as well. In this problem, increasing device size increases both average current and C_{Leff}.

f) Suppose V_{SB} = 1V, what is the value of V_{tn}, V_{tp}, V_m? How does this qualitatively affect C_{Leff}?

Solution

V_{tp} = V_{tp0} = **-0.4V.**

V_{tn} = $0.4 + \gamma \cdot (\sqrt{2\phi_F + 1} - \sqrt{|2\phi_F|})$ = **0.596** V.

Using the equation for part a) and plugging in the new value of V_{tn} gives: **V_M = 1.35V**

The increased V_{sb} will increase the depletion region and lower the junction capacitance, lowering C_{Leff}.

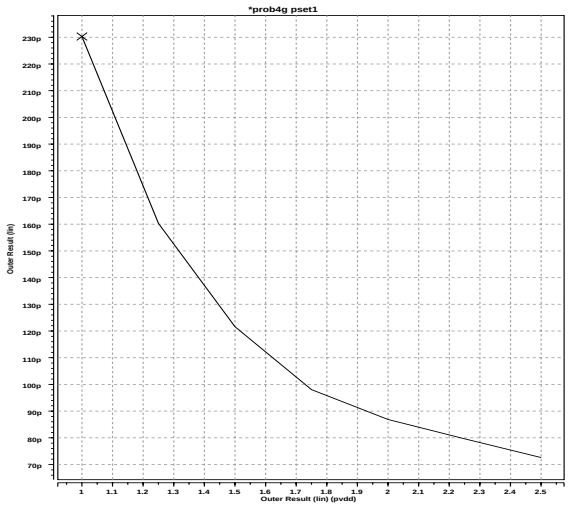
g) Use Magic to create a layout for this inverter. Extract the schematic, including parasitic capacitance, from the layout and use HSPICE to simulate the circuit and measure t_P and the average power for the

following input V_{in}: pulse(0 V_{DD} 5n 0.1n 0.1n 9n 20n), as V_{DD} varies from 1V - 2.5V with 0.25V interval. [$t_P = (t_{PHL} + t_{PLH}) / 2$]. Using this data, plot 't_P vs. V_{DD}', and 'Power vs. V_{DD}'.

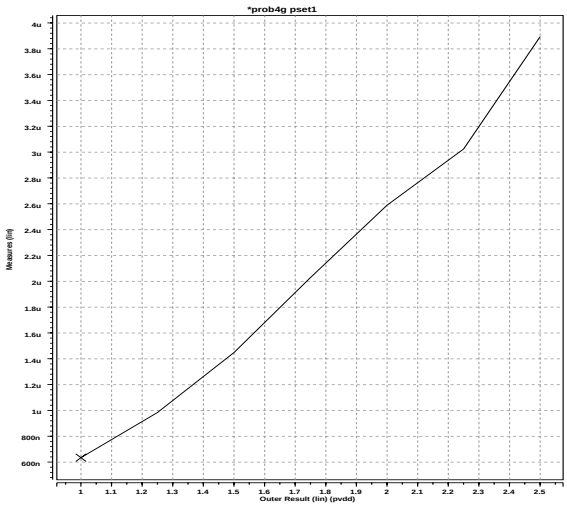
The extracted layout will include parasitics so you need not manually include AS, AD, PS, PD in your spice deck, but remember to manually add C_L = 6.5fF. Set V_{SB} = 0V for this problem. Use the **HSPICE model parameters** which can be found in " logic025.l ".

Solution

There are many valid layouts for the inverter and you can find an example in the book. For one possible layout, the simulation results are as follows. (The parasitics should be quite similar for any reasonable layout.)



Delay vs VDD (part g)



Power vs VDD (part g)

h) Using HSPICE, simulate the circuit for a set of 'pulse' inputs with rise and fall times of $t_{in\_rise,fall}$ =1ns, 2ns, 5ns, 10ns, 20ns. For each input, measure (1) the rise and fall times t_{out_rise} and t_{out_fall} of the inverter output, (2) the total energy lost E_{total}, and (3) the energy lost due to short circuit current E_{short}. For measuring short circuit power, use the technique discussed in class (slide 96, Handout 2). Use the **HSPICE model parameters** which can be found in " logic025.l"

Using this data, prepare a plot of (1) $(t_{out\_rise}+t_{out\_fall})/2$ vs. $t_{in\_rise,fall}$, (2) E_{total} vs. $t_{in\_rise,fall}$, (3) E_{short} vs. $t_{in\_rise,fall}$ and (4) E_{short}/E_{total} vs. $t_{in\_rise,fall.}$

Provide simple explanations for:
(i) Why the slope for (1) is less than 1?
(ii) Why E_{short} increases with $t_{in\_rise,fall}$?
(iii) Why E_{total} increases with $t_{in\_rise,fall}$?

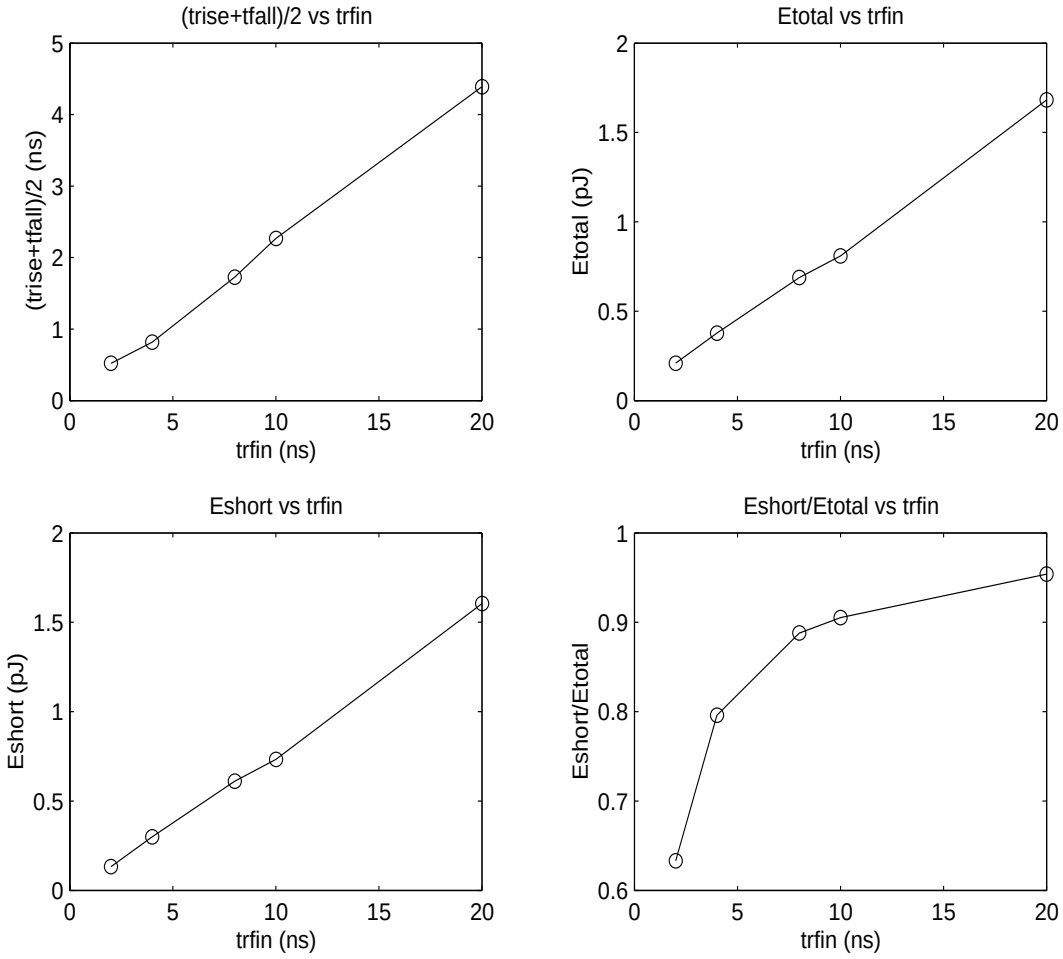
Solution

i) The slope is less than 1 because of the regenerative property of the inverter. The high gain around the

switching point causes the output to change faster than the inputs.

ii) The amount of time for which both devices are on simultaneously increases.

iii) Total energy increases because the short circuit energy begins to dominate, and it increases as the rise/fall time increases.



Plots for Problem 4(h)