Problem Set #2: Updates and Frequently Asked Questions

Notes and Hints:

Problem 6:

- *** The expression for S should be read as S=ABC+(A*notB*notC)+(notA*notB*C)+(notA*B*notC). If you interpreted it the as A*not(BC) etc and have already completed the layout we'll accept that, but please complete the other parts of the problem for the correct interpretation of S.
- This should read just "transmission gate", not "NMOS transmission gate" You may assume inputs and their complements are available as inputs.
- For part c, the sizing should be W/L=0.5/0.25u for all NMOS and W/L=2u/0.25u for all PMOS.