Low-Power High-Speed Links

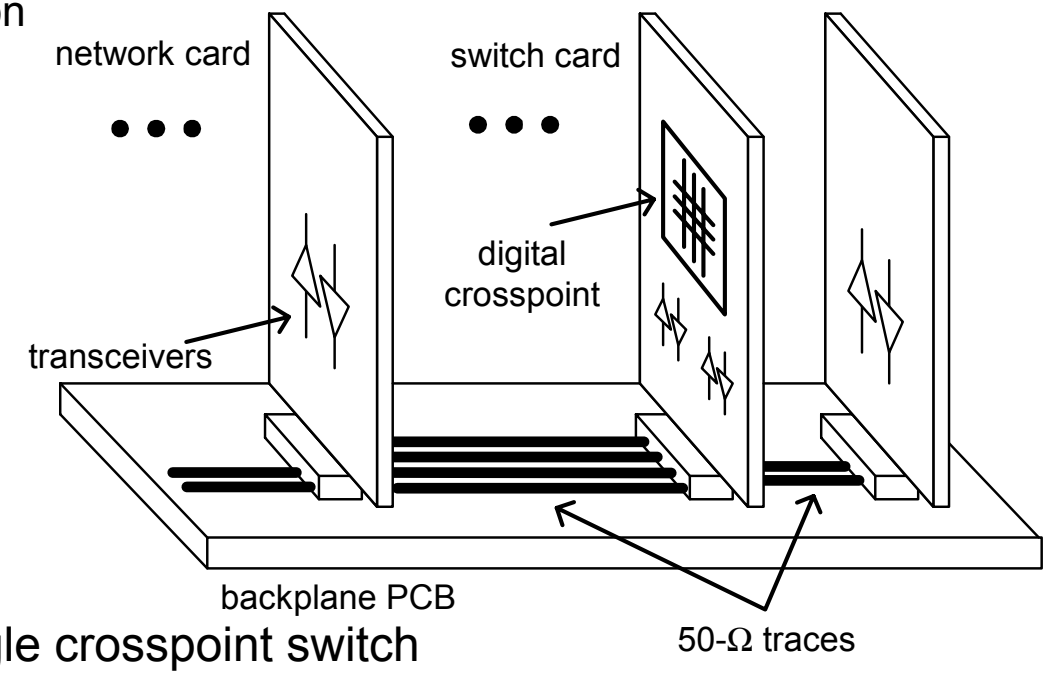
Gu-Yeon Wei
Division of Engineering and Applied Sciences
Harvard University
6.976 Guest Lecture, Spring 2003

Outline

- Motivation
- Brief Overview of High-Speed Links
- Design Considerations for Low Power
- DVS Link Design Example
- Summary

Motivation

- Demand for high bandwidth communications
- Advancements in IC fabrication technology
  - Higher performance
  - More complex functionality
  - → Chip I/O becomes performance bottleneck
  - → Increasing power consumption
- Network router example



- 10's to 100's of links on a single crosspoint switch

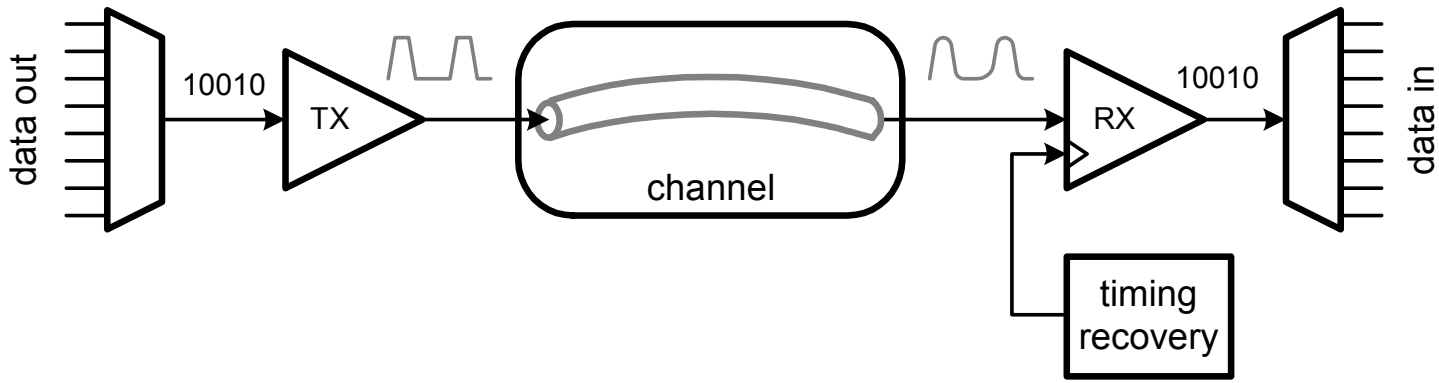
High-Speed Links Overview

- High-speed data communication between chips across an impedance controlled channel
  - Shared communication bus (memories)
  - Point-to-point links
- Types of link architectures and implementations
  - Parallel vs. serial
  - Differential vs. single-ended
  - Low-impedance vs. high-impedance driver
  - Transmitter-only vs. receiver-only vs. double termination

- We will focus on point-to-point serial links using differential high-impedance drivers with double termination for network routers
  - Techniques to reduce power applicable to other link types

Link Components

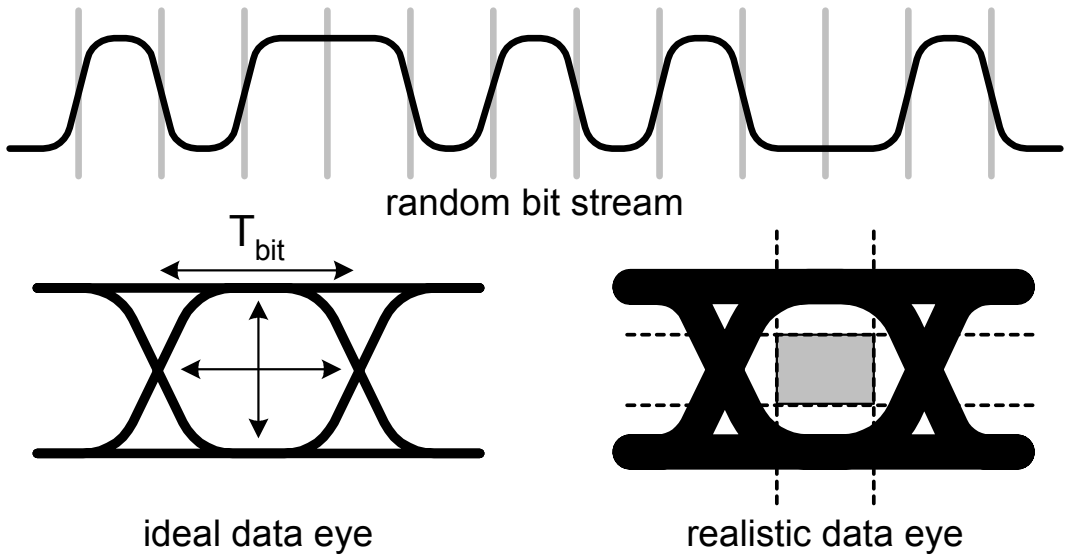
- High-speed links consist of 4 main components



  - Serializing transmitter driver
  - Communication channel
  - De-serializing receiver samplers
  - Timing recovery

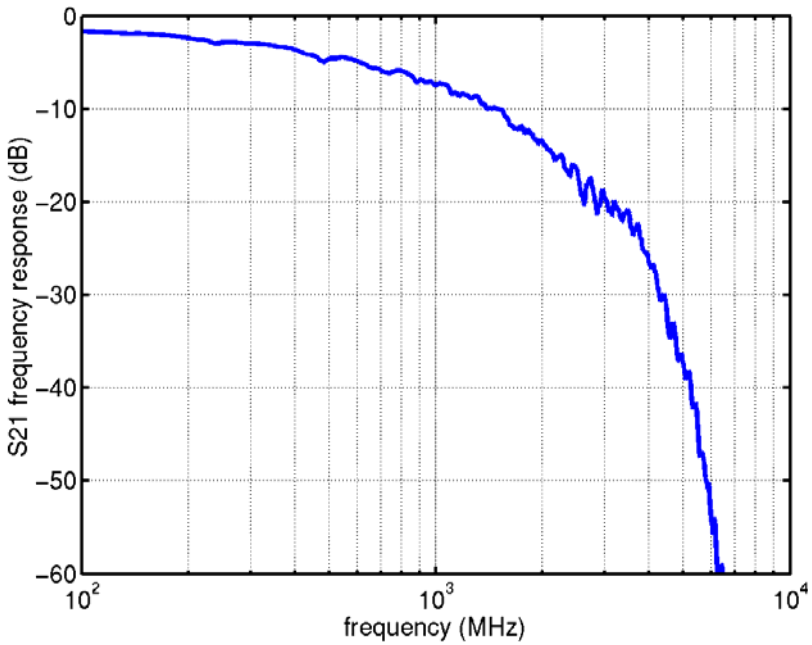
Performance Limitations

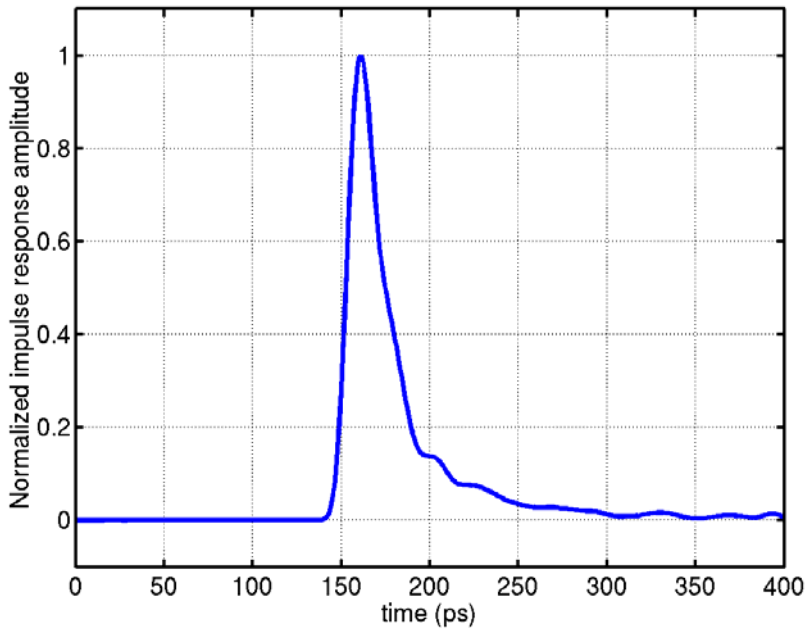
- Important to look at performance because higher performance can lead to lower power by trading off performance for energy reduction
- Several factors limit the performance of high-speed links
  - Non-ideal channel characteristics
  - Bandwidth limits of transceiver circuitry
  - Noise from power supply, cross talk, clock jitter, device mismatches, etc.
- Eye diagrams – a qualitative measure of link performance



Channel Impairments and ISI

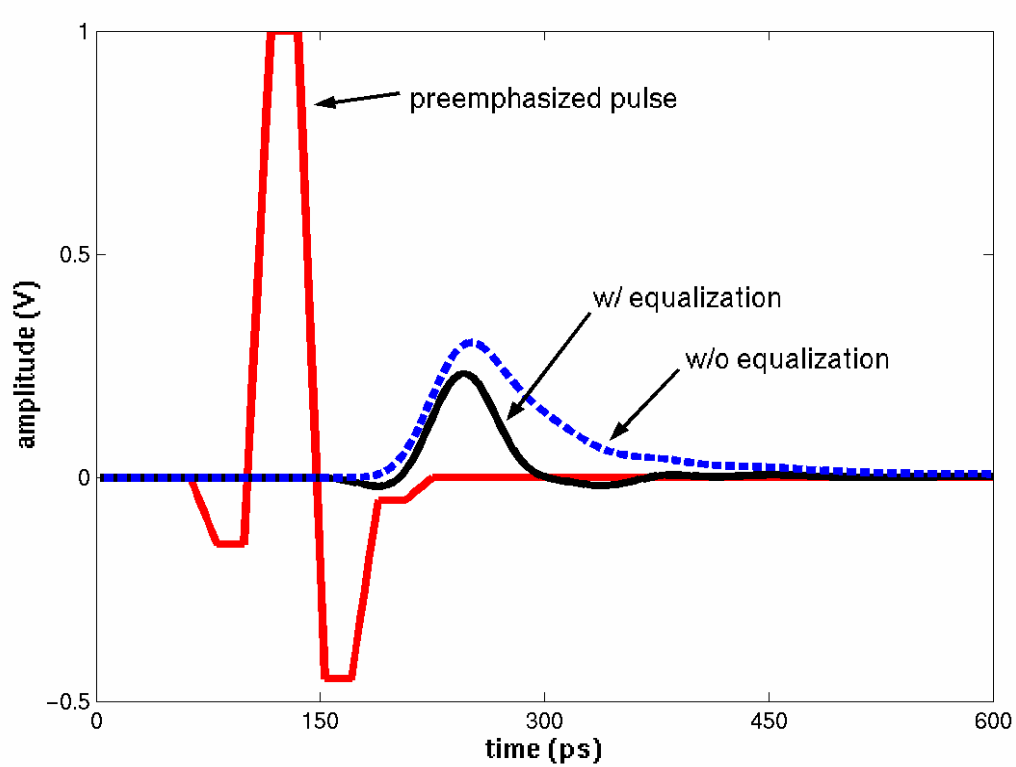
- One of the dominant causes of eye closure is inter-symbol interference (ISI) due to channel bandwidth limitations
  - Two ways to view channel impairments





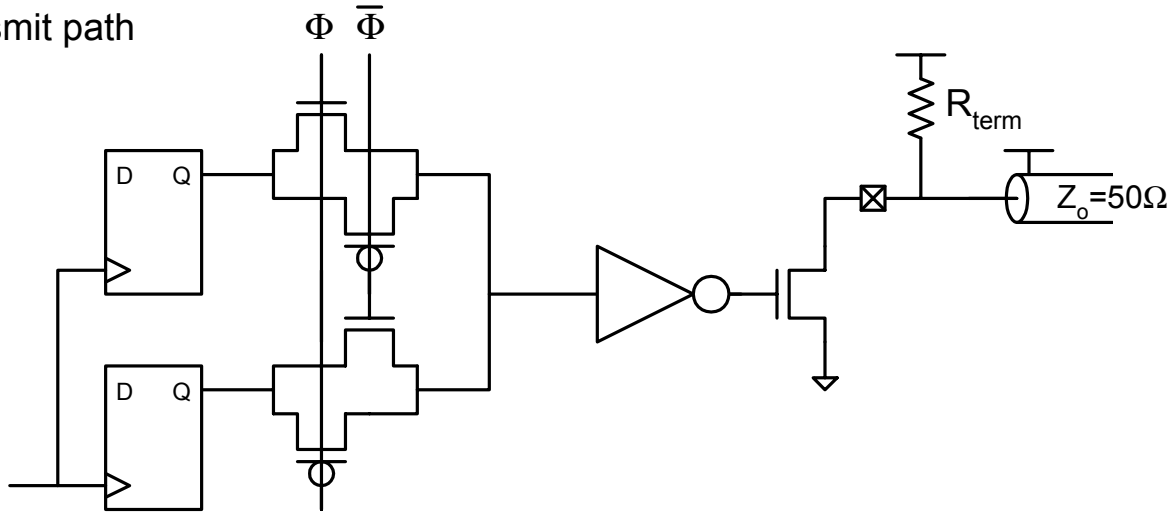
Equalization

- Placing a high-pass filter in the signal path can counter the roll-off effects of the channel
  - Preemphasis or transmit-side equalization is commonly used

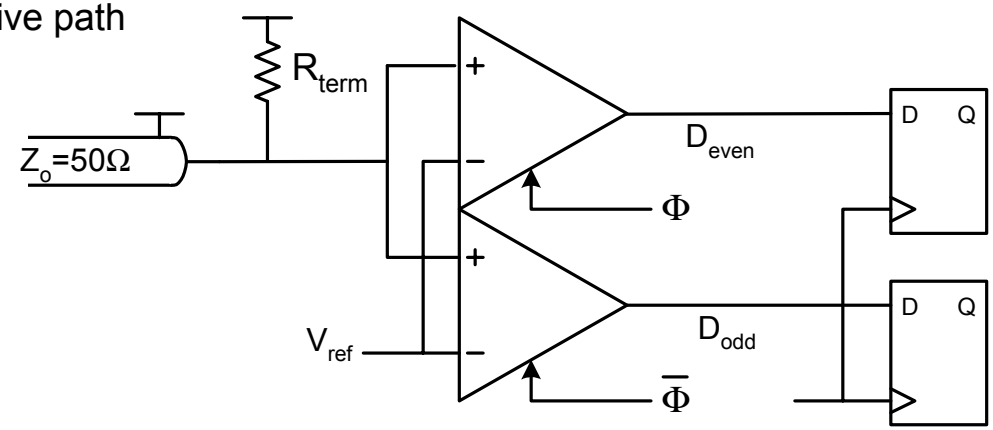


Critical Path in Links

- The critical path in links can be as short as 1~2 gate delays
  - Transmit path

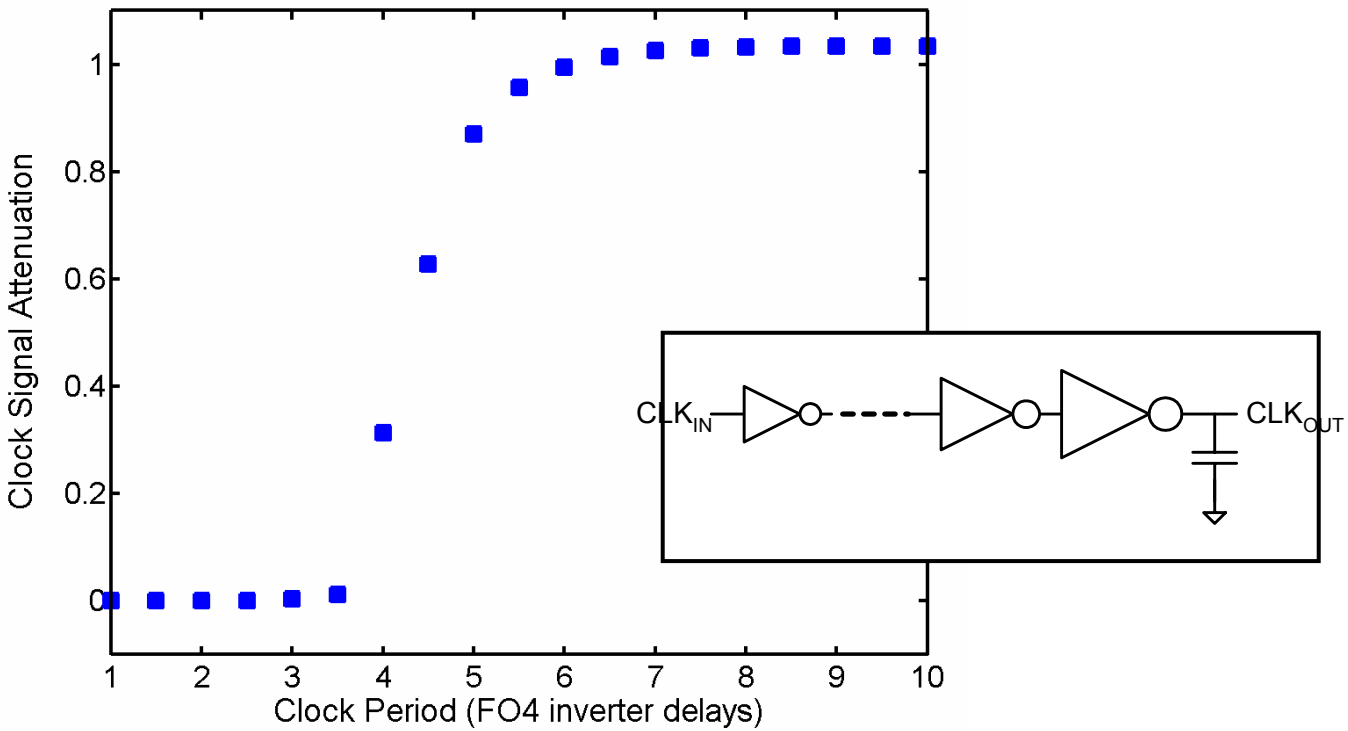


  - Receive path



Clock Frequency Limit

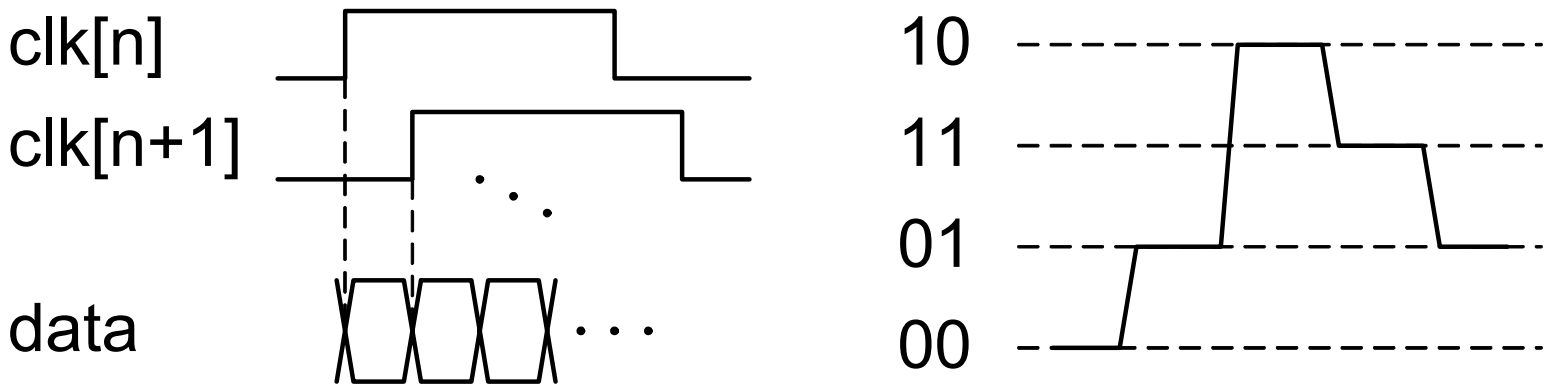
- While a symbol time can be short, there is a limit to the maximum on-chip clock frequency
  - Must distribute a clock driven by a buffer chain



- Overcome this limitation with parallelism

Parallelism

- Parallelism can increase bit rate even with limited clock frequency
  - Time-interleaved multiplexing
  - Multi-level signaling



- Some performance issues to be wary of
  - Static timing offsets in multi-phase clock generator (DLL or PLL)
  - Requires higher voltage dynamic range in transmitter and receiver
- Parallelism can also be low power

Sources of Noise

- Power supply noise
  - Translates into voltage and timing uncertainty
- Cross talk
  - Near- and Far-End Cross Talk (NEXT and FEXT)
  - High-frequency coupling
- Clock Jitter
  - Timing uncertainty in transmitted and sampled symbol
  - Probabilistic distribution of timing edges (bounded and unbounded components)
- Device mismatches and systematic offsets
  - Deterministic or systematic variation in timing edges from multi-phase clock generators

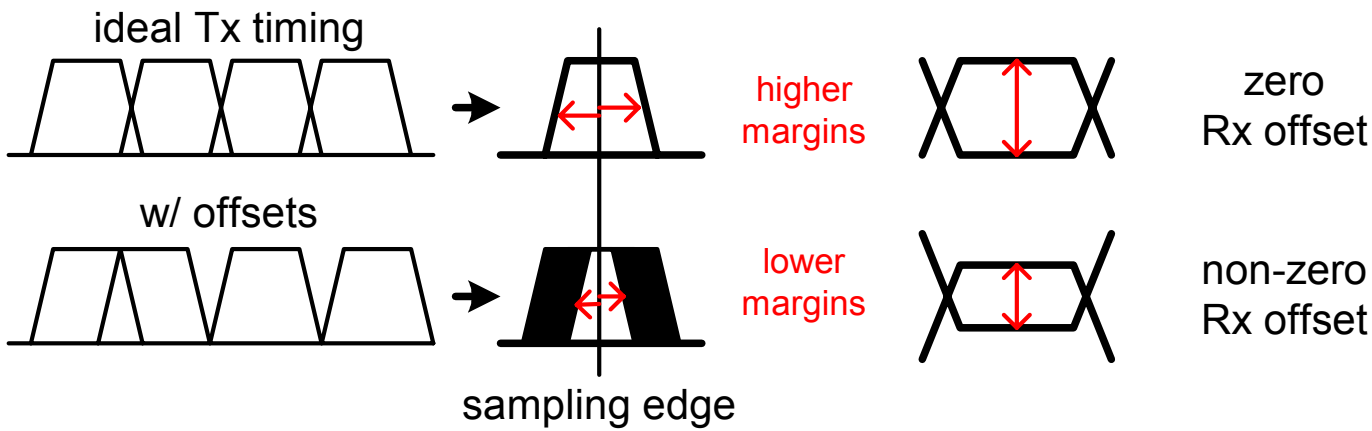
Considerations for Low Power

- Low noise → low power
  - Target some signal to noise ratio (SNR)
  - Reducing noise allows for lower signal power
- Trade speed for lower power
  - Reducing bit rate improves SNR
  - Many noise sources are fixed → ratio of timing uncertainty to bit time improves (have longer bit times)

- Let's look at a few design choices for low power
  - Circuit level
  - Architecture level
  - System level

Offset Calibration

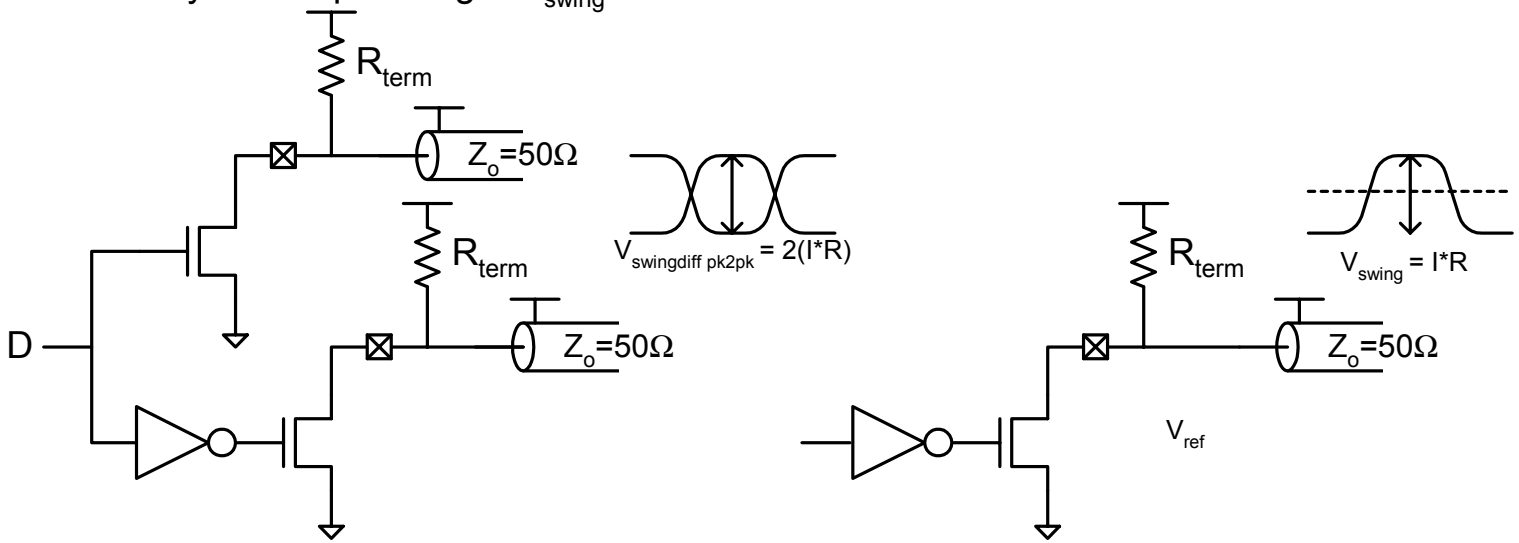
- Two sets of offsets that can manifest itself as voltage and timing uncertainty to close the eye and may require higher power to overcome them:
  - Multi-phase clock generator timing offsets
  - Receiver input voltage offsets



- Static offsets due to systematic (layout) and random (device) mismatches
  - Calibration enables more timing and voltage margins (i.e., lower noise)

Differential Signaling

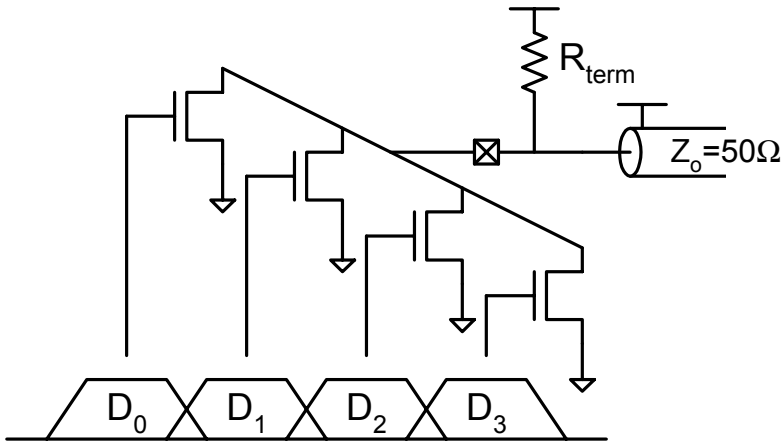
- Differential communication can lead to a lower power solution
  - Immunity to common mode noise
  - Injects less noise into the supplies
- But aren't there now are two channels that switch? Yes, but…
  - Signal amplitudes can be smaller on both channels
  - Alternative is pseudo-differential signaling but needs a reference voltage which can be noisy and require larger V_{swing}

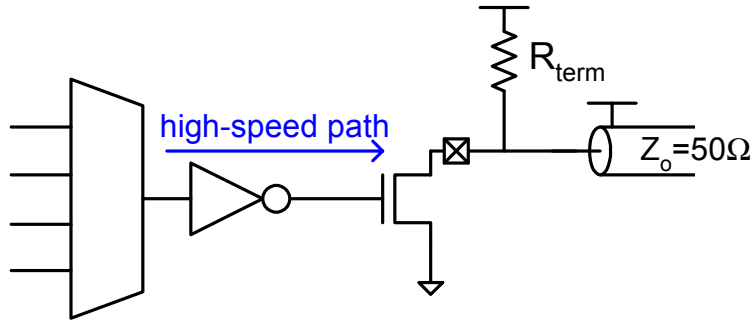


- What does it cost?
  - Requires two pins per link

Signal Multiplexing

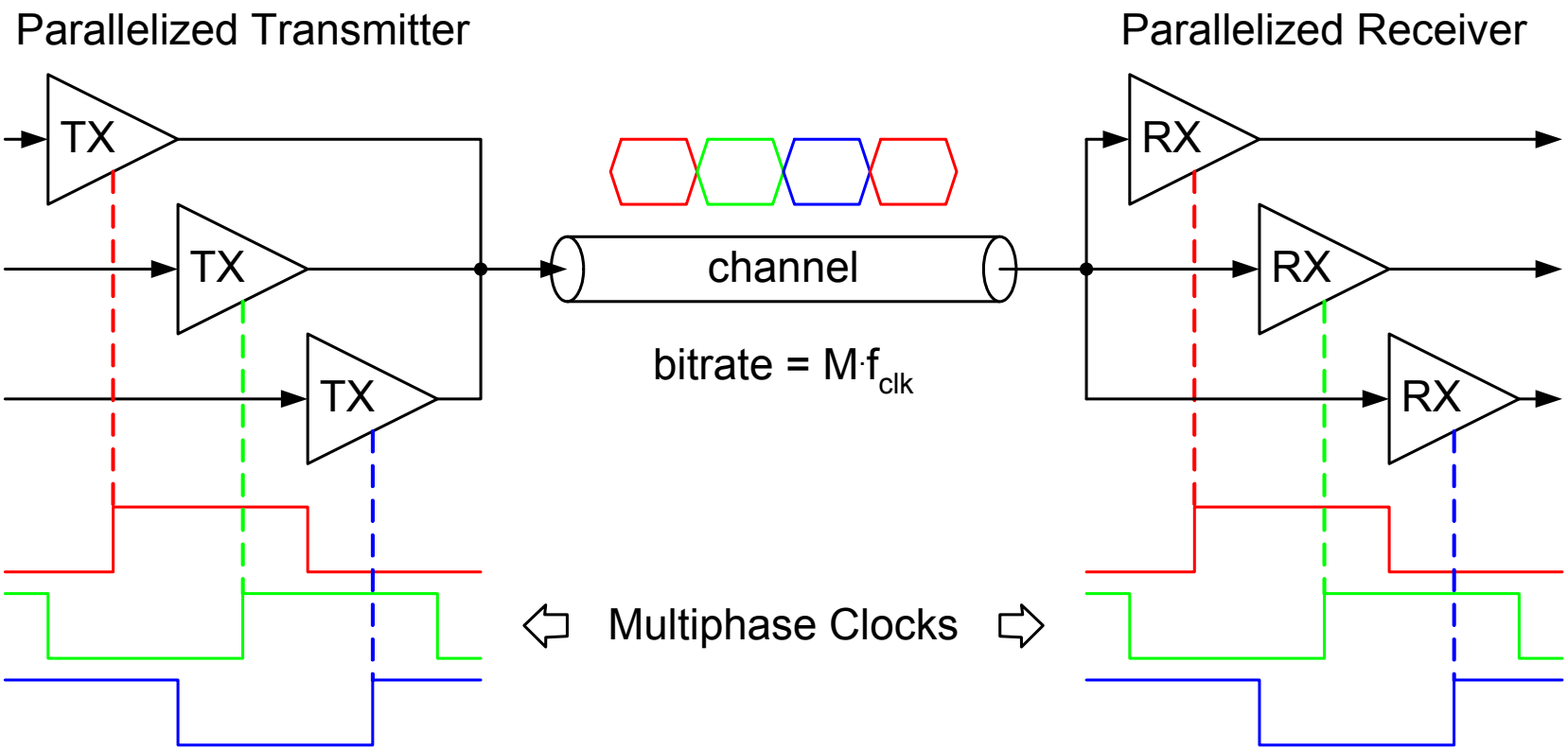
- There are different options for choosing where to combine pulses to create sub-clock period symbols
  - Combine at the final transmitter stage vs. farther up stream





  - C_{load} for the clocks higher when combined at the final transmitter vs.
  - Need faster signal path after the multiplexer
- Best choice depends on implementation (see Zerbe, ISSCC2003)

Multiplexing



Multiplexing = Low Power?

With M:1 multiplexing, f_{CLK} = bit rate/M

- Power = $M \cdot CV^2 \cdot f = M \cdot CV^2 \cdot (BR/M) = C \cdot V^2 \cdot BR$

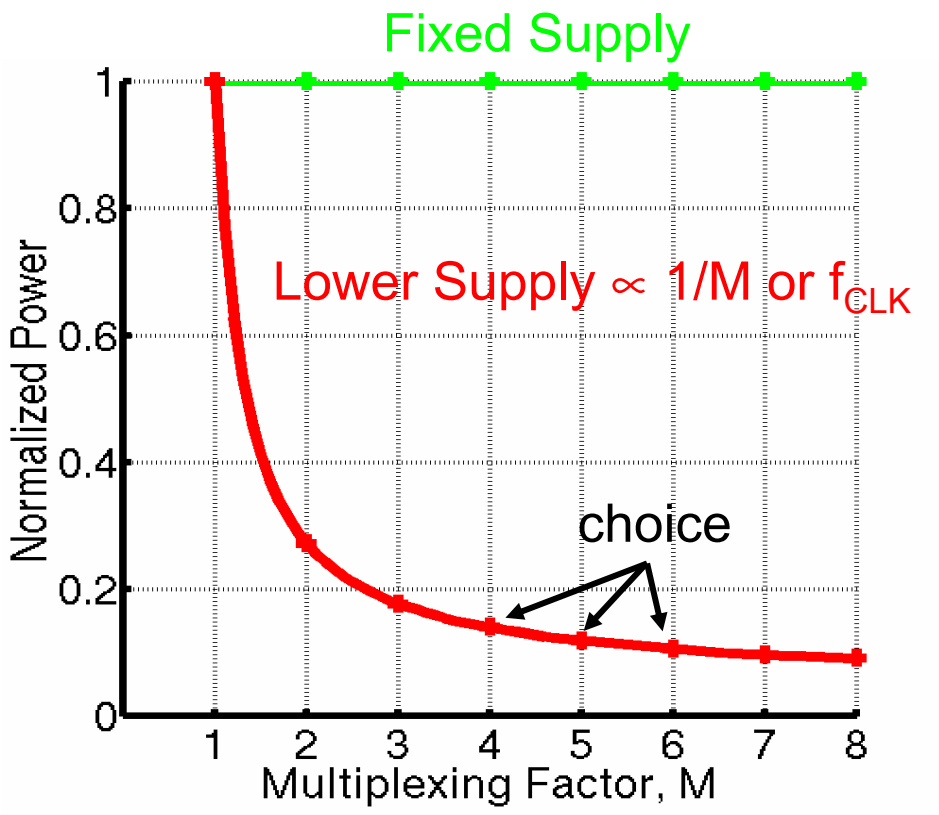
- With fixed supply, power does not vary with M

But wait, at lower frequencies, I can lower voltage!

- With lower supply voltage ($V \propto f_{CLK} = BR/M$),
- Power decreases as $\propto 1/M^2$!

Power vs. M

- Larger M
- ⇨ Can reduce voltage
- ⇨ Lower power
- ⇨ Less accurate timing
  - static phase offsets
  - jitter
- Cannot make M arbitrarily large b/c there is a lower limit to Vdd
- Choice: M= 4~6



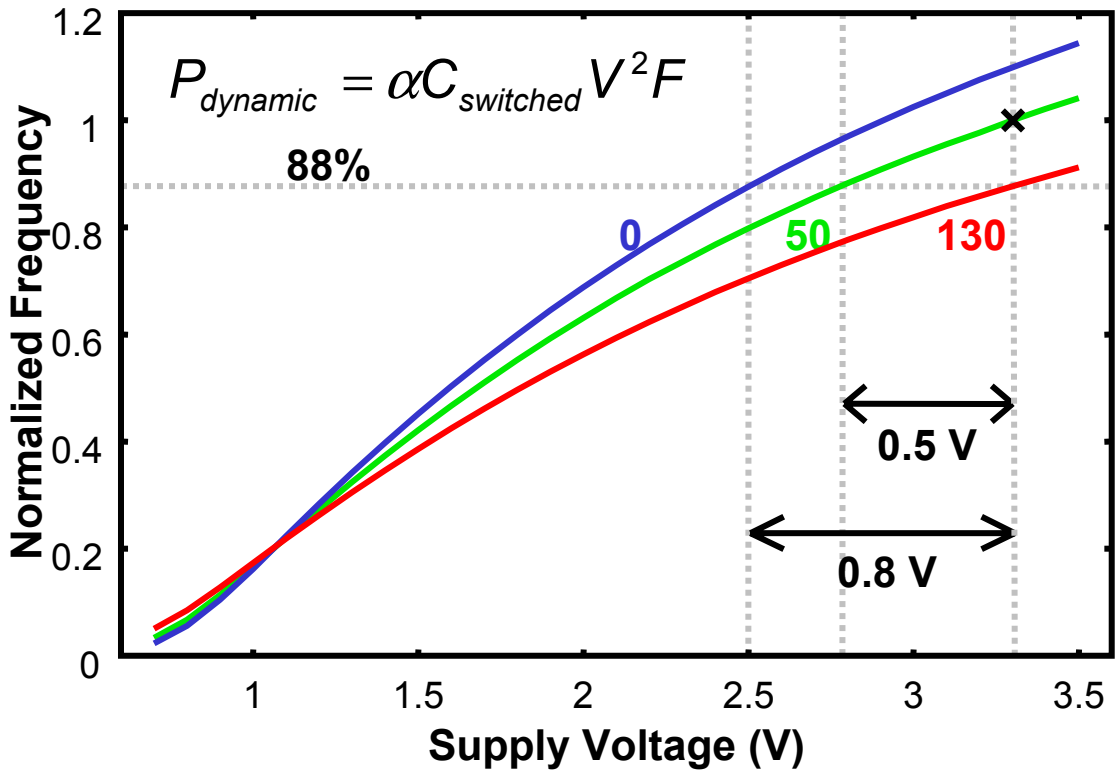
This begs the questions… What if we make Vdd adaptive w/ f_{CLK}?

DVS Links

- Dynamic Voltage Scaling (DVS)
  - Technique first introduced for digital systems (e.g., uP, DSP chips)
    - Lot's of work done in both academia and industry (e.g., Intel, Transmeta)
  - Allows trade off between speed and power
- Let's investigate DVS for high-speed links
  - Motivation and potential benefits
  - Design example from Dr. Jaeha Kim (ISSCC2002, JSSC2002, PhD thesis 2002)

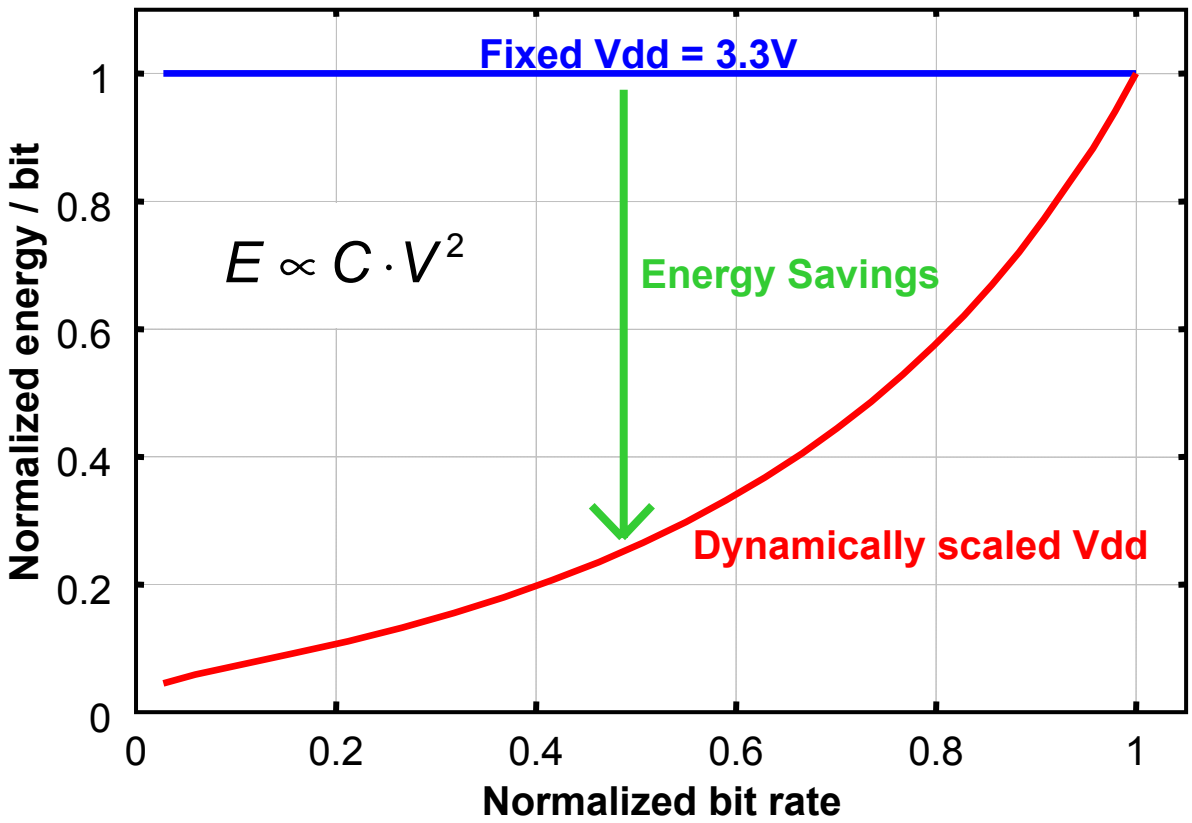
DVS Links

- Dynamic Voltage Scaling (DVS) can reduce power consumption in two ways
  1) Digital circuits operate at their most energy-efficient point in the presence of PVT variations by eliminating extra performance margins



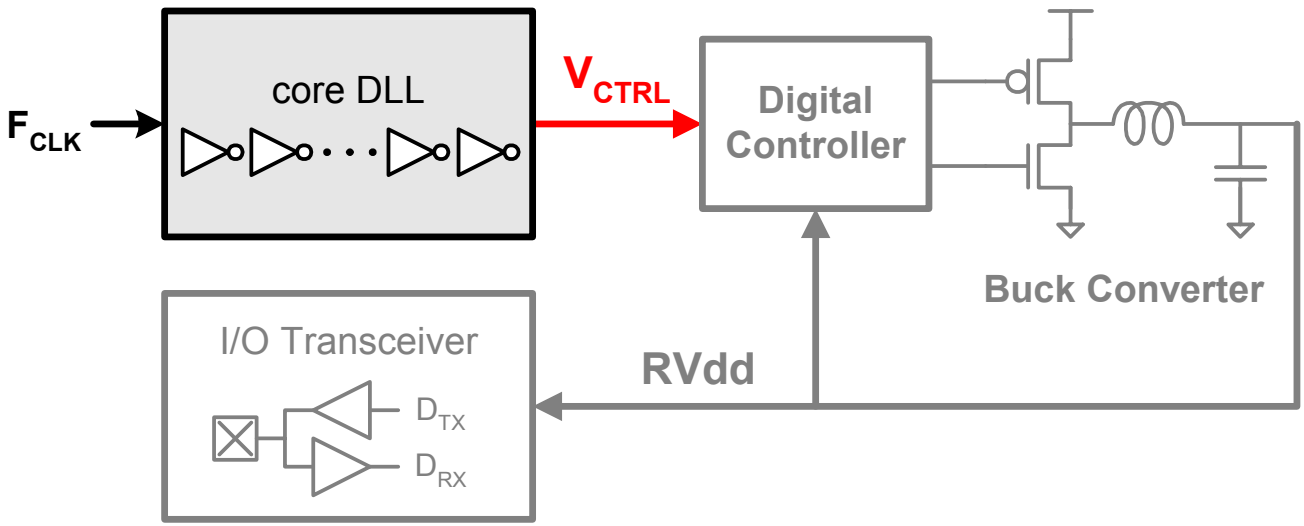
Trade Performance for Energy Savings

2) DVS enables trade off between performance and energy
   - Reducing frequency alone reduces power but not energy per bit

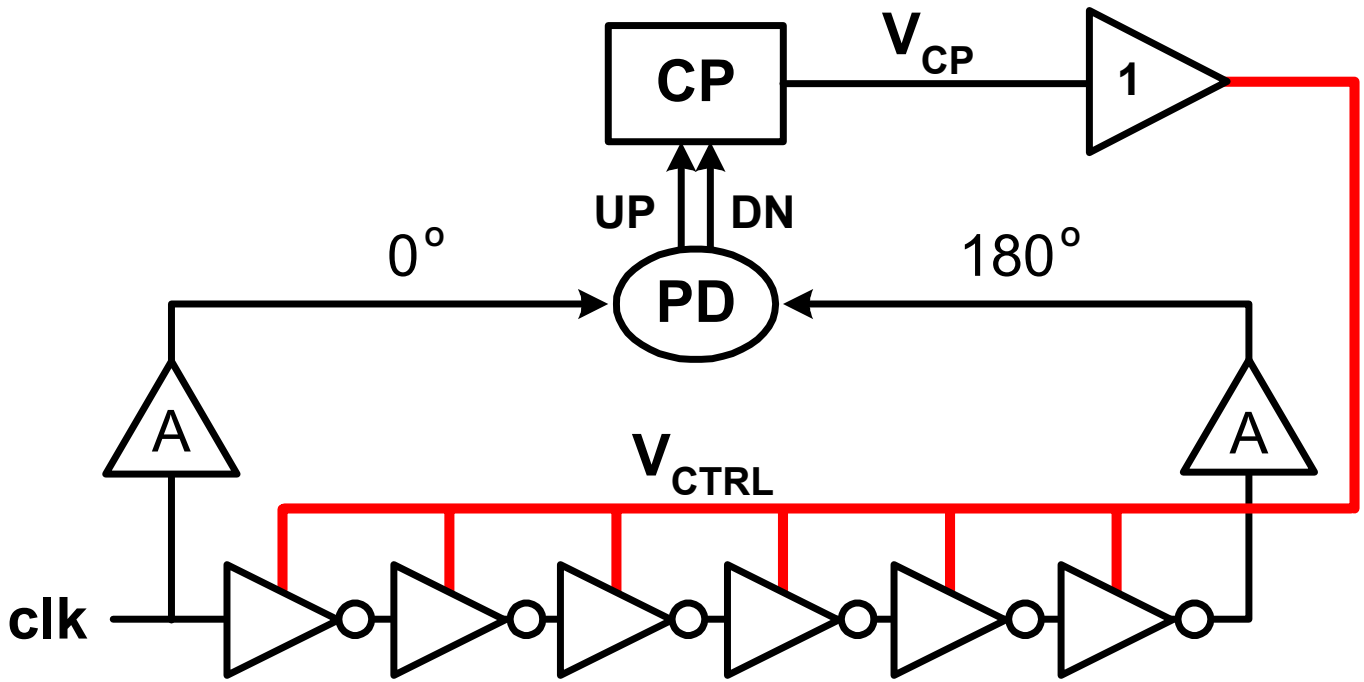


DVS Link Components

- DVS links require two additional components
  - Mechanism to measure circuit critical path to appropriately adjust voltage with respect to frequency
    - Use an on-chip performance monitor circuit (inverter delay elements of core DLL)
  - Efficient supply-voltage regulator (buck converter)
- Overall Block diagram (Wei *et al*, ISSCC2000)



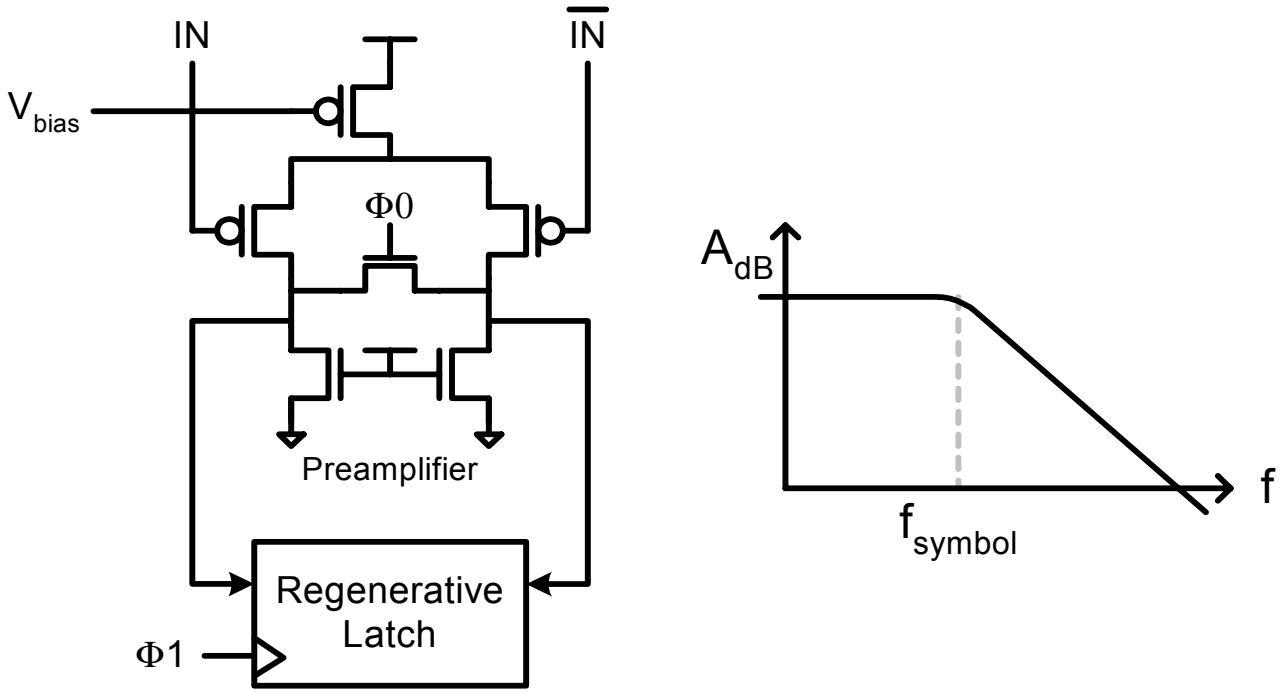
Performance Monitoring DLL



- Reduces design complexity by enabling one to replace precision analog components with simple digital gates. How?
  - Inverters of the delay line model the critical path (clock distribution)
  - Delay of gates in I/O circuitry are fixed relative to clock period

Adaptive Receiver Filter

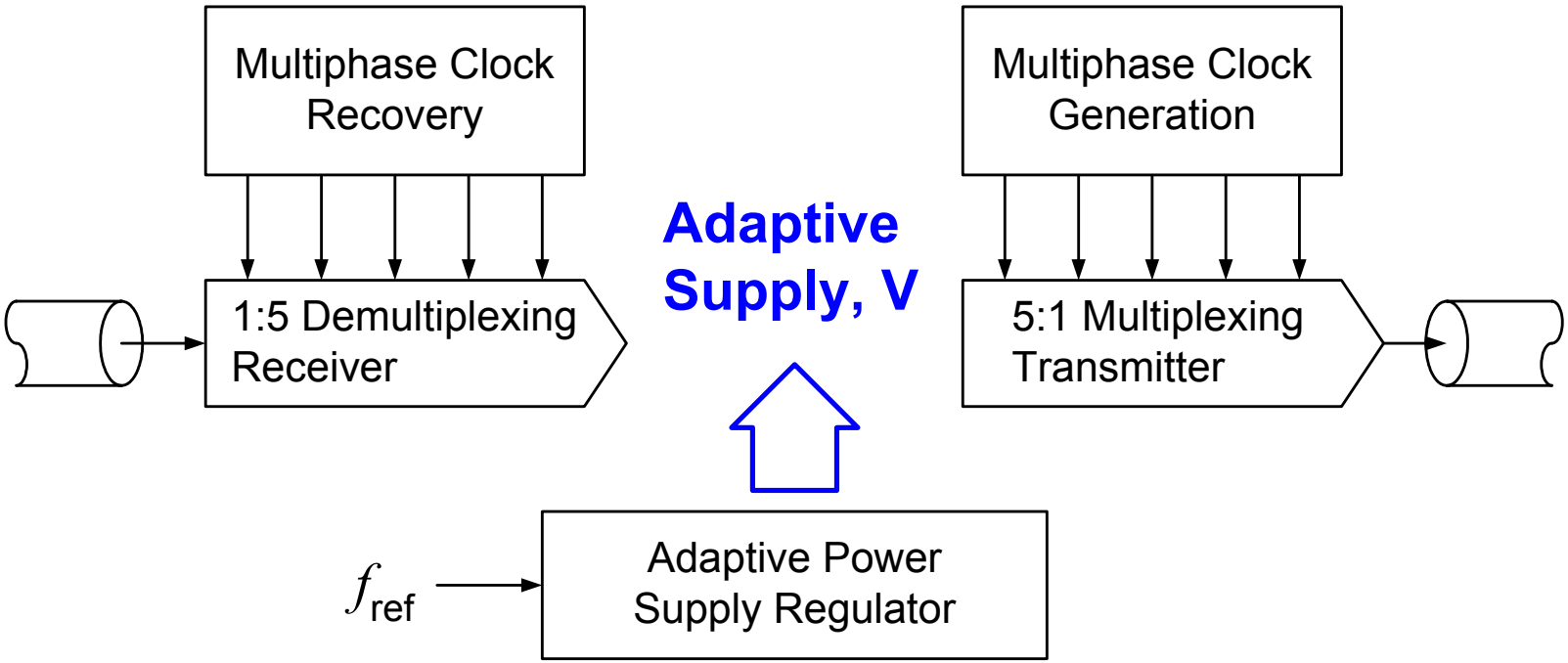
- Filter signal frequencies beyond the Nyquist rate at the receiver (helps for dealing with cross talk)
- Receiver example



  - Filter's corner frequency tracks f_{symbol}

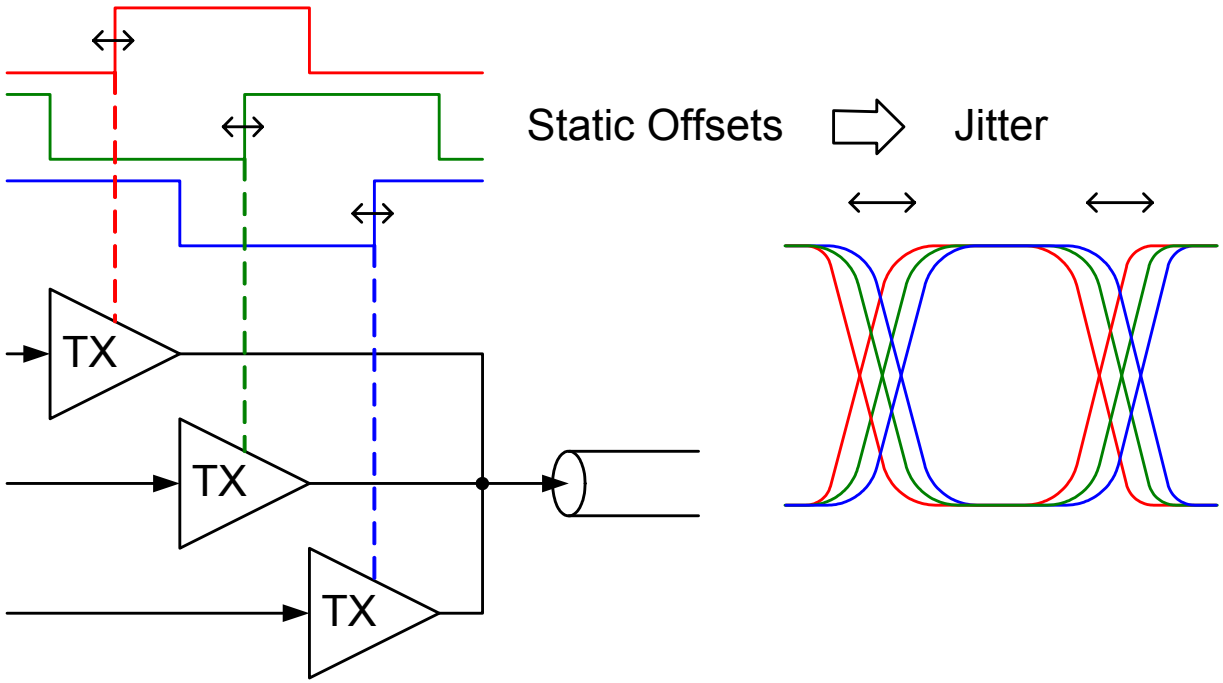
Example: Adaptive Supply Serial Links

- Jaeha Kim (Ph.D. defense 2002)

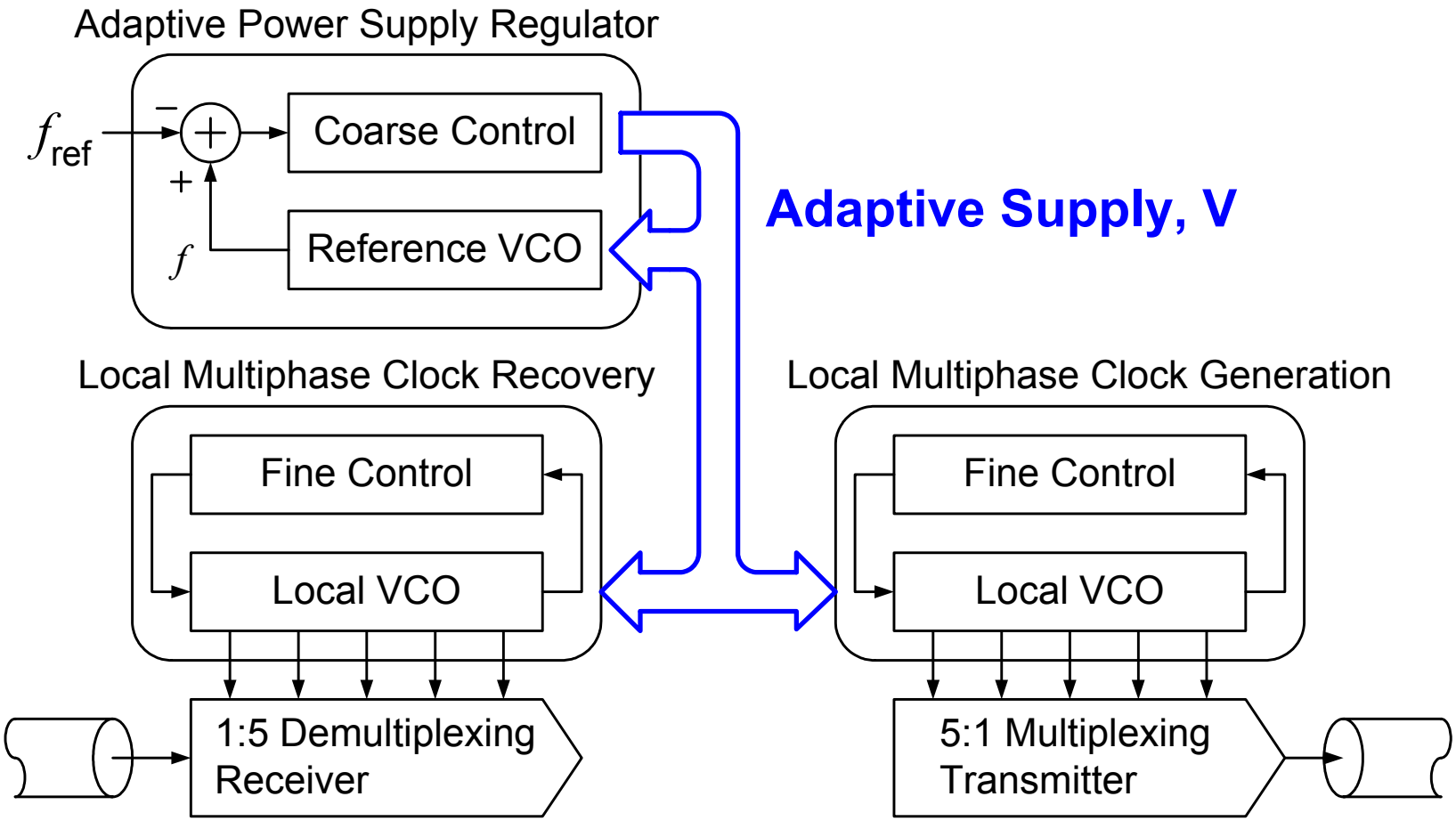


Multi-Phase Clock Generation

- Must minimize static offsets between phases
- Generate multiphase clocks locally at each pin, but watch out for power and area overhead



Dual-Loop Clock Generation

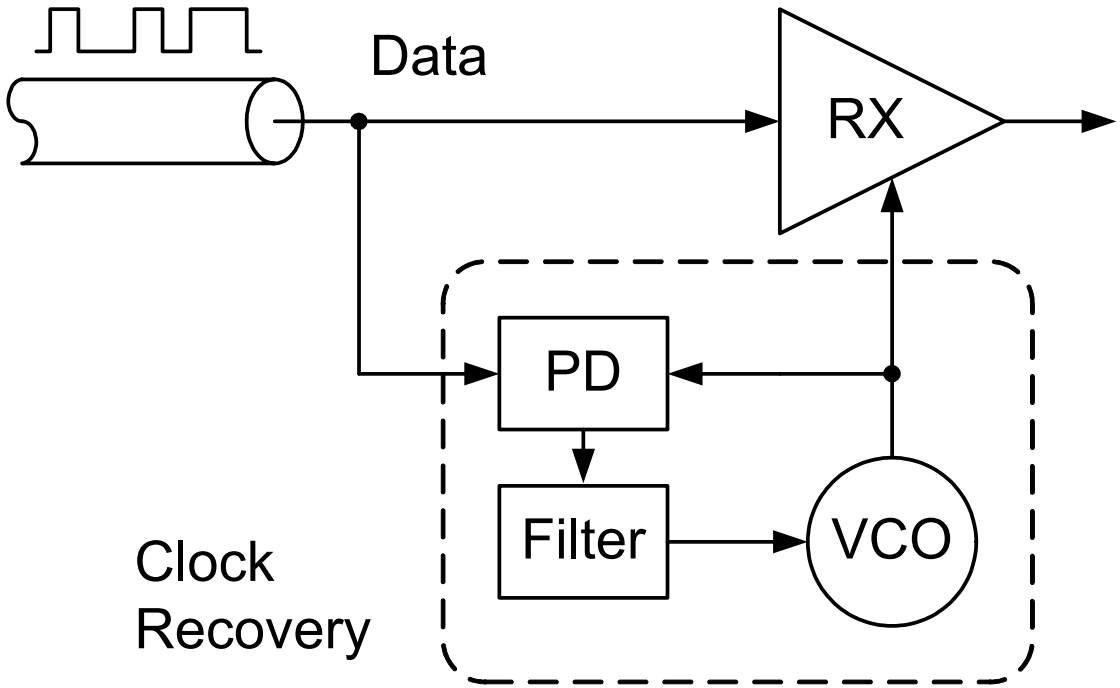


Dual-Loop Clock Generation (2)

- Global loop brings the local VCO frequency close to lock
- Narrow local tuning range (+/-15%) is sufficient to compensate for on-chip mismatches
- Narrow tuning range leads to low VCO gain
  - Small loop capacitor area (2.5pF)
  - Low sensitivity on Vctrl noise

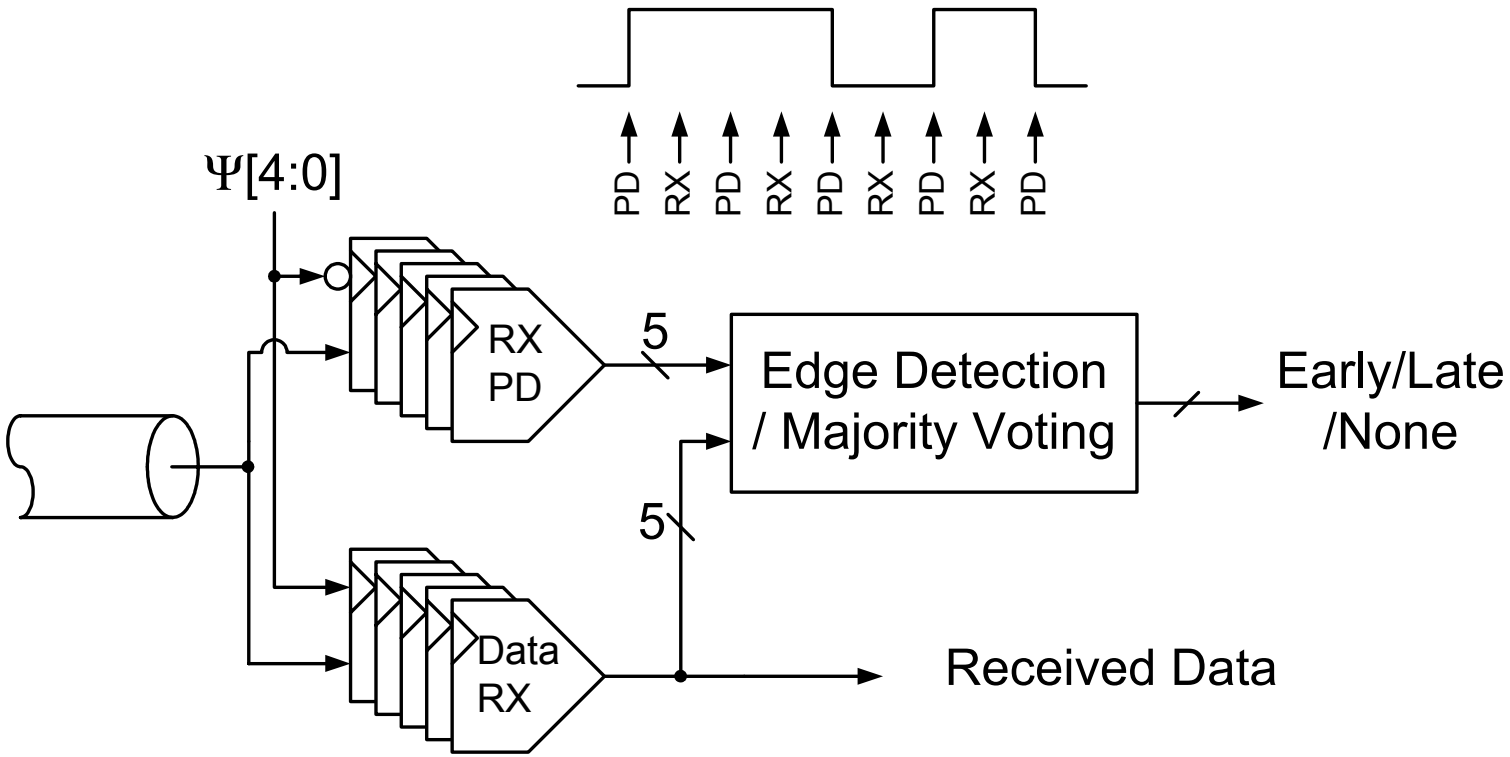
Clock Recovery

- Optimal receiver timing is recovered from the incoming data stream



Phase Detection

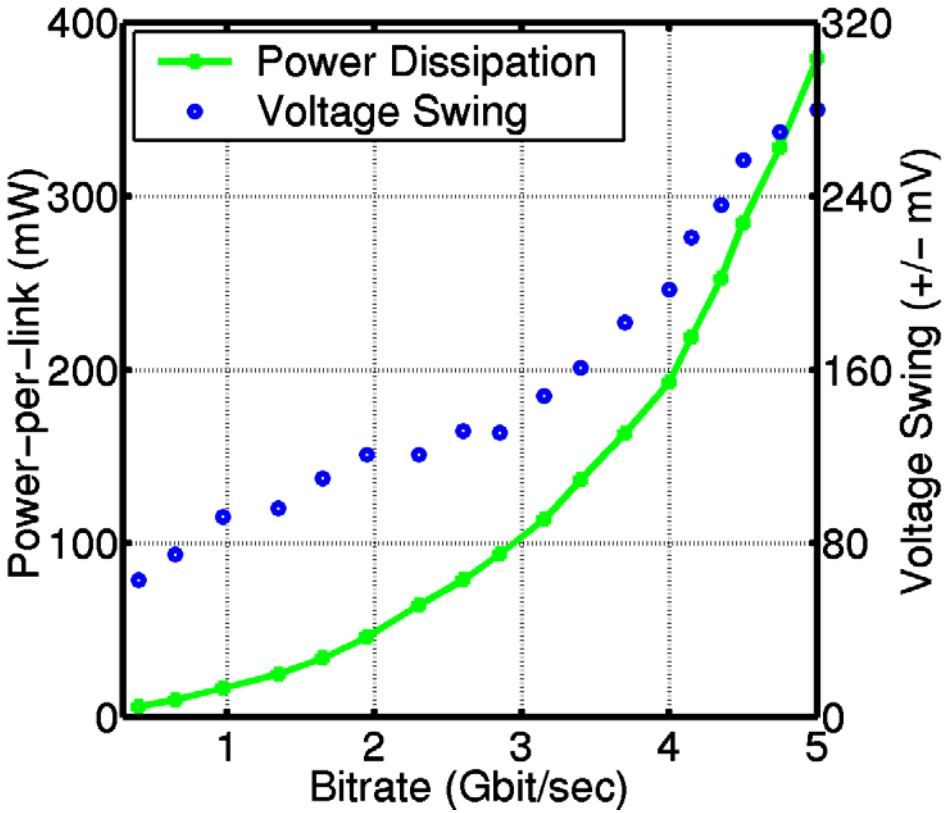
- Phase detector made of an identical set of receivers minimizes timing error

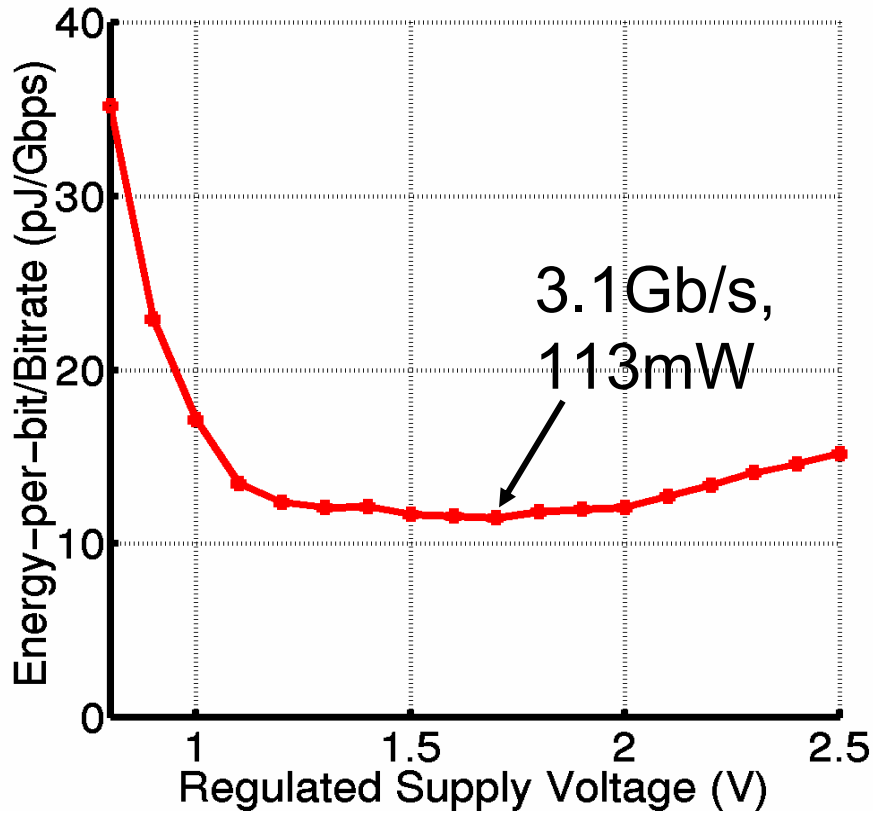


Chip Prototype

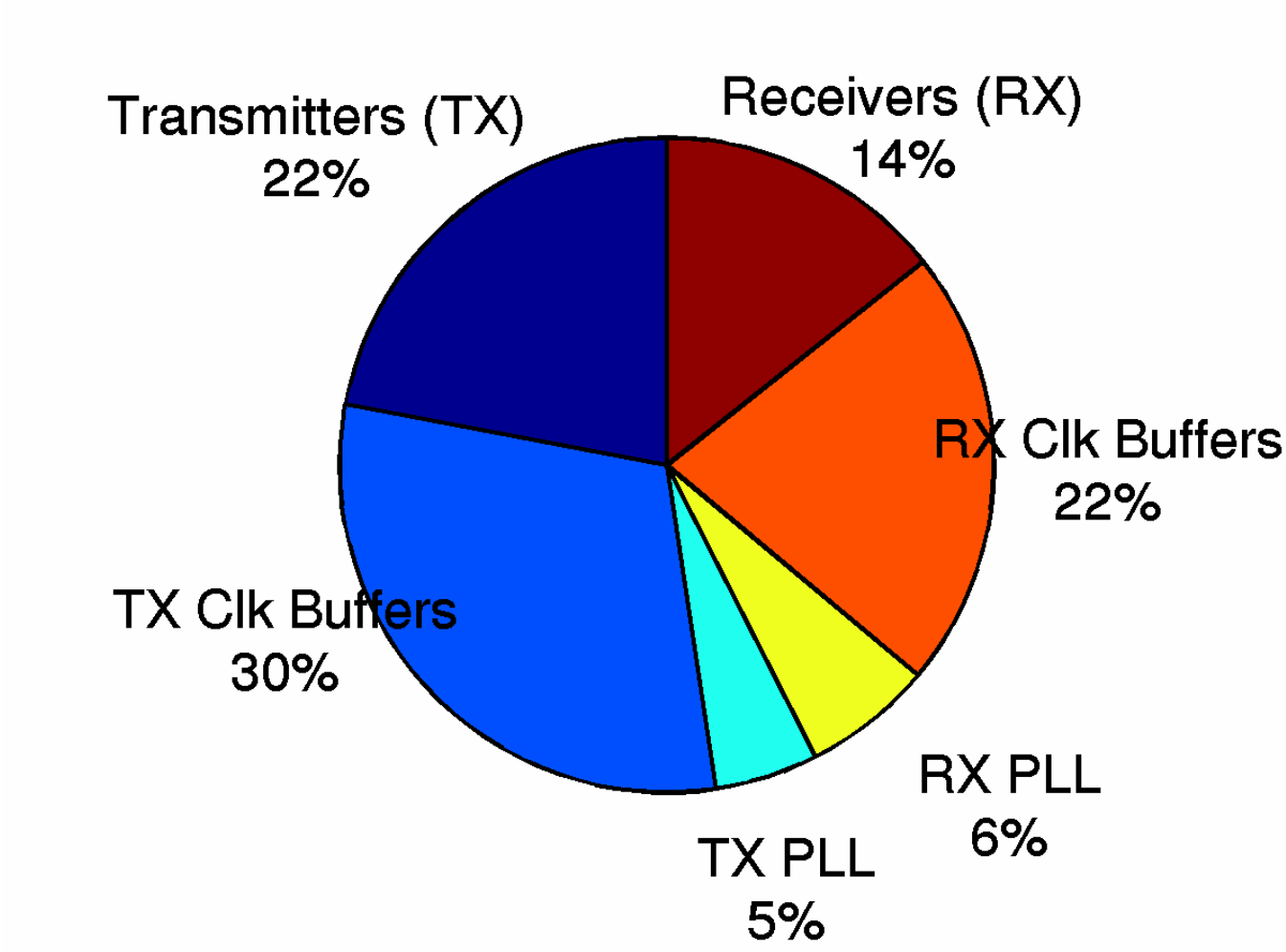
- 0.25μm CMOS
- 2.5V / 0.55Vth
- $3.1 \times 2.9 mm^2$
- 0.4~5.0Gb/s
- 0.9~2.5V
- 5.6~375mW
- BER < 10^{-15}
- Reg. Efficiency: 83-94%

Power and Performance





Power Breakdown



Summary

- Higher performance links require low noise → low noise solutions lead to lower power
  - Trade performance (speed) for power reduction
- DVS links enable energy-efficient link operation and also have some nice properties
- Outstanding issues with using DVS links
  - Communication during frequency and voltage transitions
  - Supply voltage regulator slew rate limits
  - Overhead of multiple regulators