ESD.290 Special Topics in Supply Chain Management
Brian Subirana & Sanjay Sarma, MIT

History



- 1998: DISC founded
- 1999: Auto-ID Center founded Auto-ID Field Trial started 2000
- 2001: First standards presented
- 2002: Gillette orders 500,000,000 tags from Alien
- 2003: Wal-Mart, DoD Mandates EPCglobal launched, Center retired
- 2004: More mandates

Outline

- RFID and the Auto-ID Center
- An in-depth look at some issues



Outline, Part I

- RFID and the Auto-ID Center
 - What and why of RFID
 - The cost issue
 - Manufacturing low-cost RFID
 - Handling the data
 - Current status
- An in-depth look at some issues



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Magnitude of Challenges

• Inventory Management:

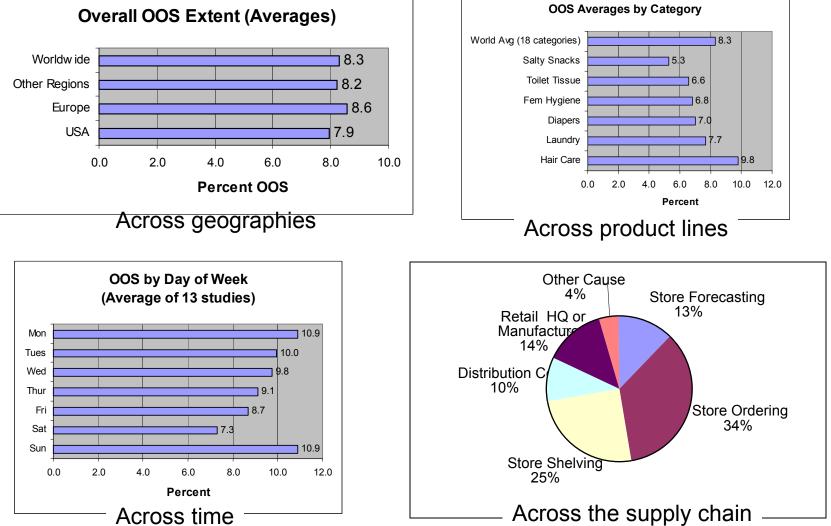
- Inventory uncertainty:
 - 65 % of 370,000 records inaccurate (HBS study of one major retailer)
 - Transportation uncertainty: Perfect delivery is dismal
- Stock-outs:
 - Average 9% out of stock in retailers world-wide
 - Lost sales due to stock-outs: 4%
- Overstock: Huge channel inventories
 - CPG average 11 weeks inventory
 - Retailers average 7 weeks inventory
 - Locked up capital, industry-wide

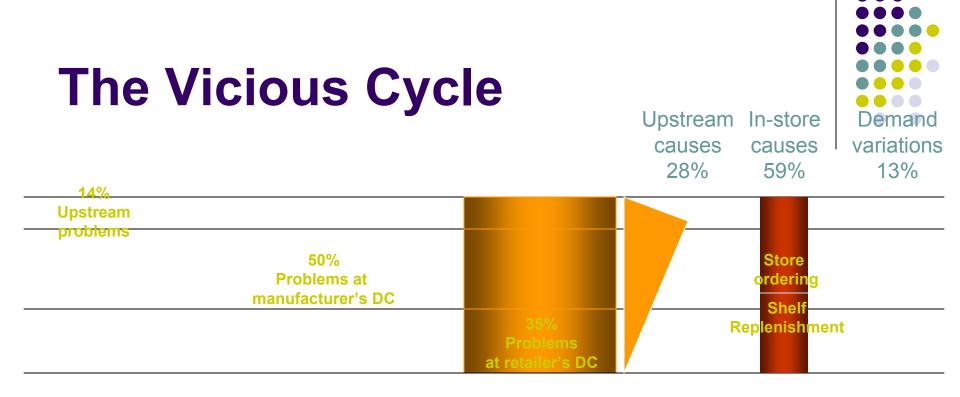
• Brand Management:

- Counterfeit:
 - \$500B pharmaceuticals business, \$50B counterfeit
- Diversion:
 - Market size difficult to estimate



The problems are everywhere

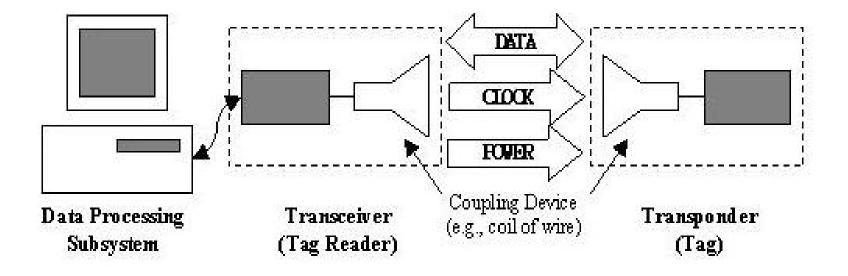


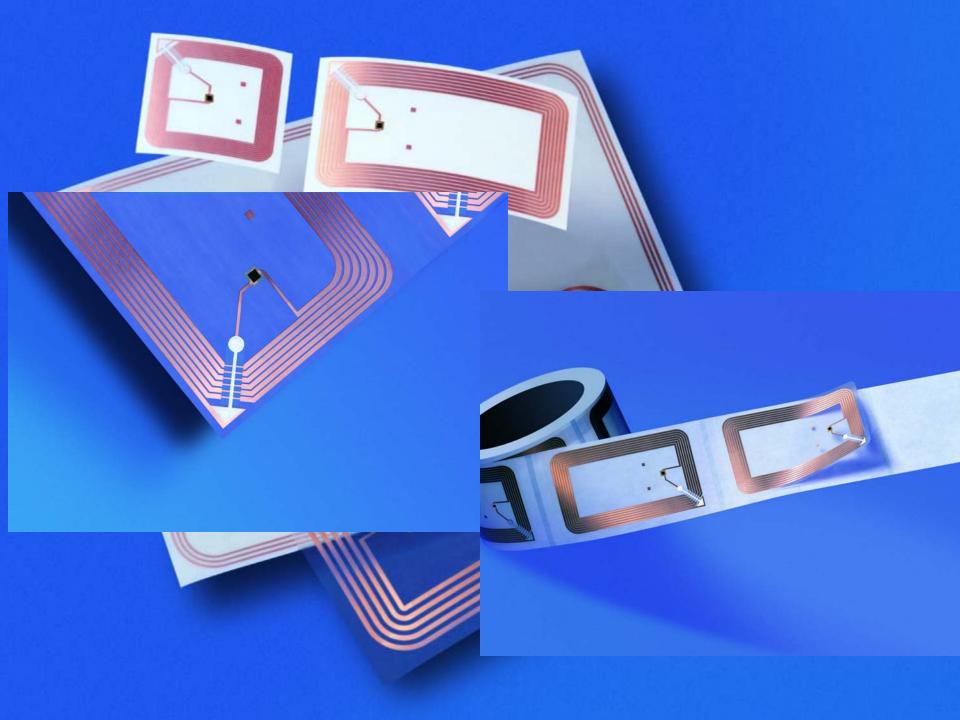




RFID System

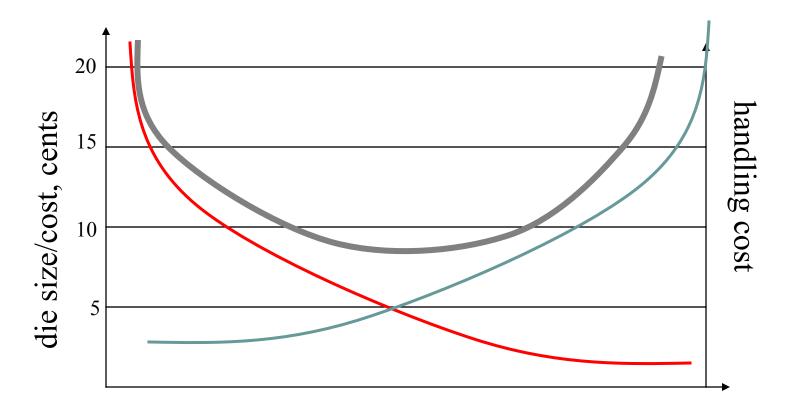






Low cost rfid

Silicon: 4c/mm²

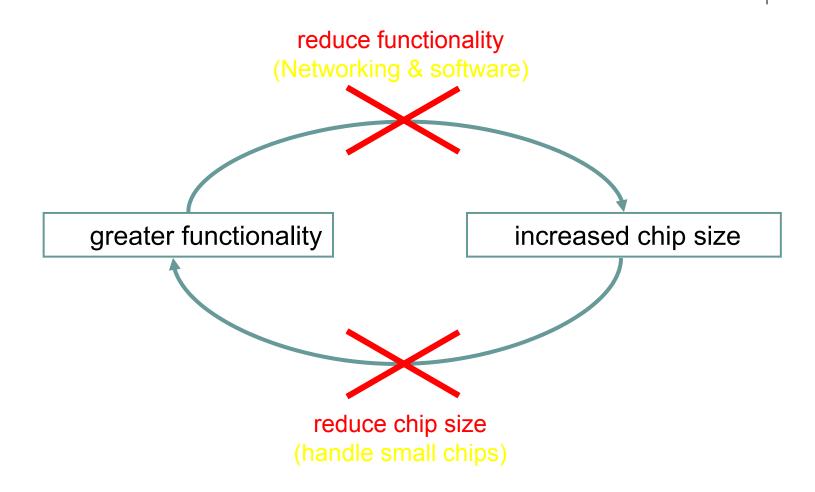




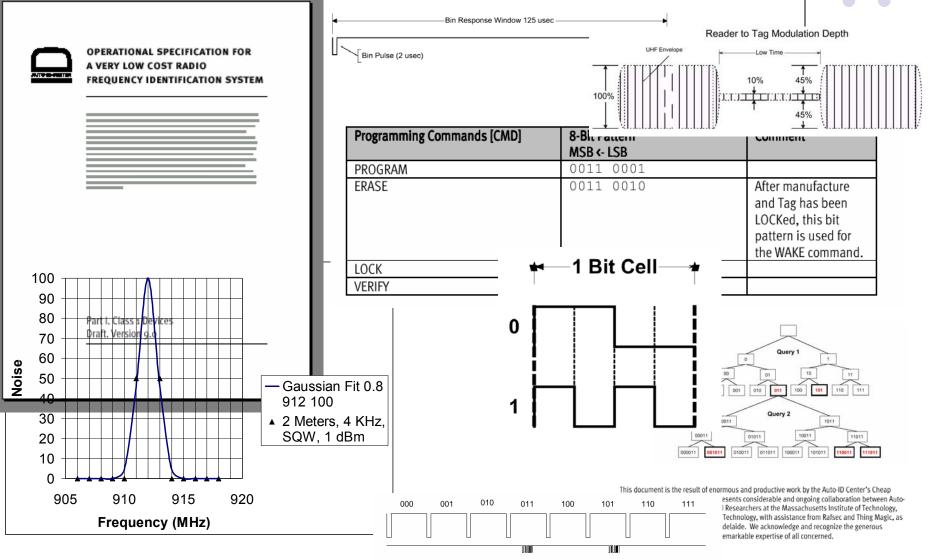
time



Why is RFID expensive today?



Cheap protocol



the hypothesis or bet

- Place unique number on tag
 - Electronic Product Code, EPC
 - 64 bit, 96 bit, and upwards

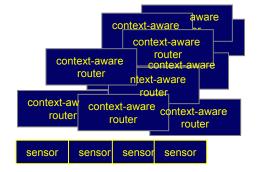
 Develop manufacturing technology for small chips and tags

Move data on the network

- Network service for resolving EPC
- Network architecture for gathering and routing data







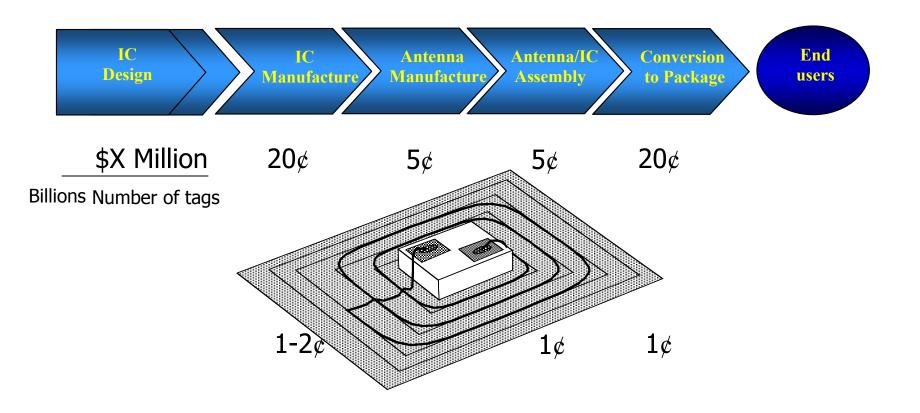
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Low cost RFID



Challenges of IC minimalism

• 0.25 mm²: does it make life tougher?

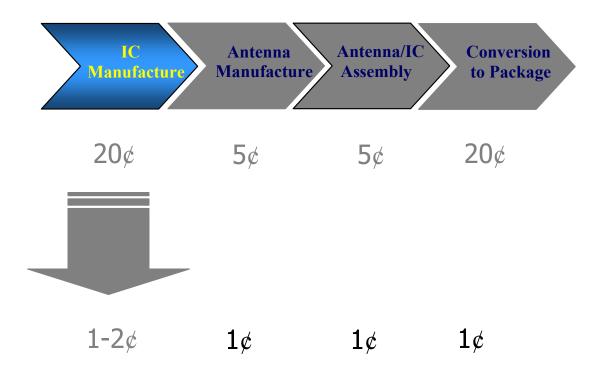
.

- Street width will dominate
- Still have to test the IC's (?)
- Die handling costs are high
- Die-attach/wire-bonding techniques do not scale
- Street width will dominate
- Still have to test the IC's (?)
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low cost rfid challenges



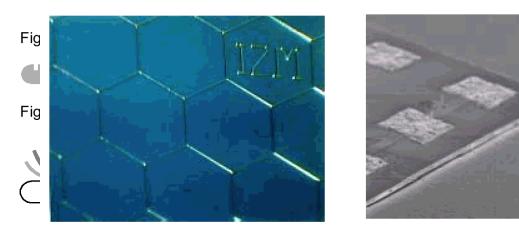
Testing

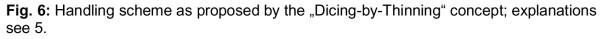
- Economics today:
 - \$500 \$1000 per wafer
- But minimal functionality means
 - High reliability
 - Don't test on wafer
 - Test wirelessly at conversion



Slicing and Dicing

- Standard saw-dicing wasteful
- Instead, use separation by thinning





C. Landesberger, S. Scherbaum, G. Schwinn, H. Spöhrle: "New Process Scheme for Wafer Thinning and Stress-free Separation of Ultra Thin IC's," Proceedings of Microsystems Technologies 2001, Mesago, Stuttgart, pp. 431-436, 2001.

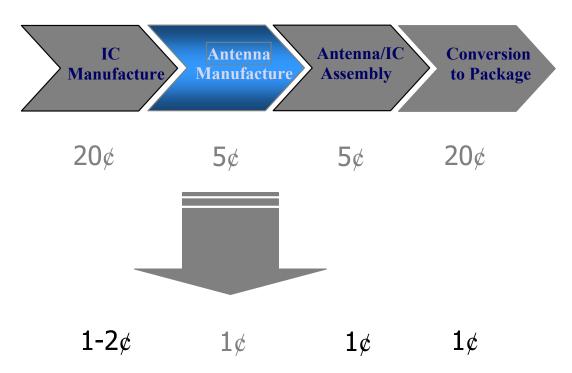


Wafer Thickness

Index Depth of Ca



Low cost RFID challenges



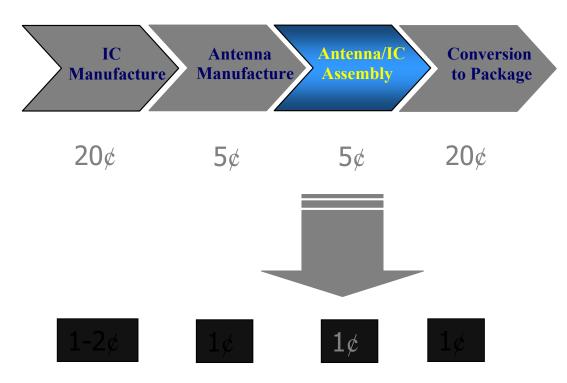
Antenna

- Screen printing
- Etching
- Forming





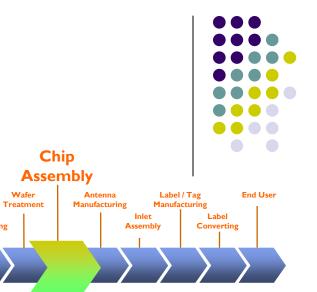
Low cost RFID challenges



Assembly

- Fluidic Self Assembly
- Vibratory Assembly
- Pick and place





Chip

Design

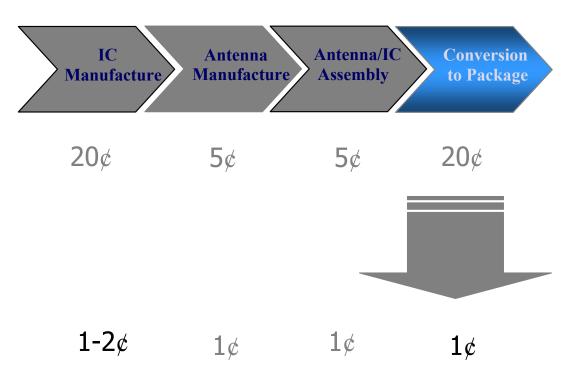
Silicon

Manufacturing

Vibratory Assembly

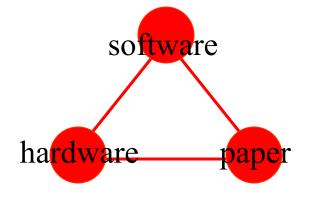


Low cost RFID challenges



Conversion

- Paper/package/label industry expertise
- Scales well with mass production
- Capital equipment expenditure





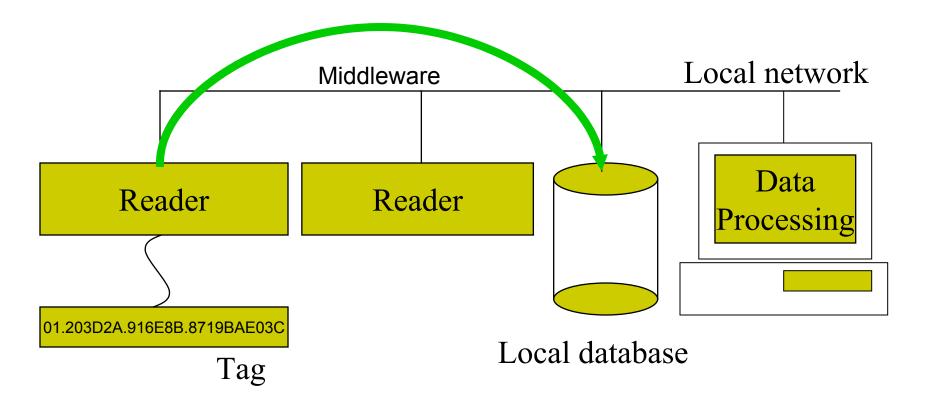
Outline, Part I

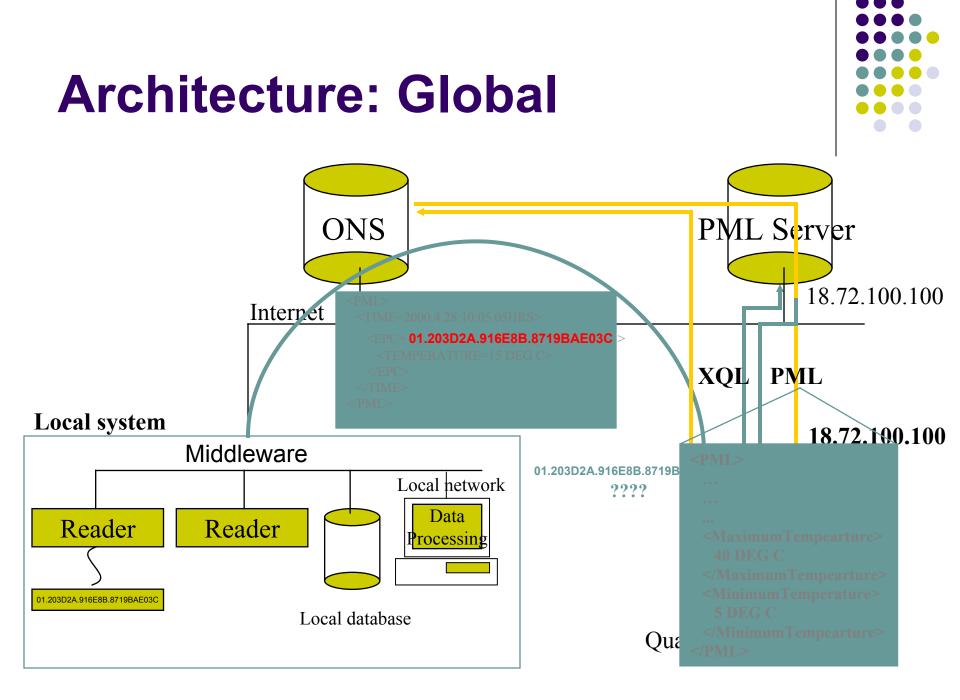
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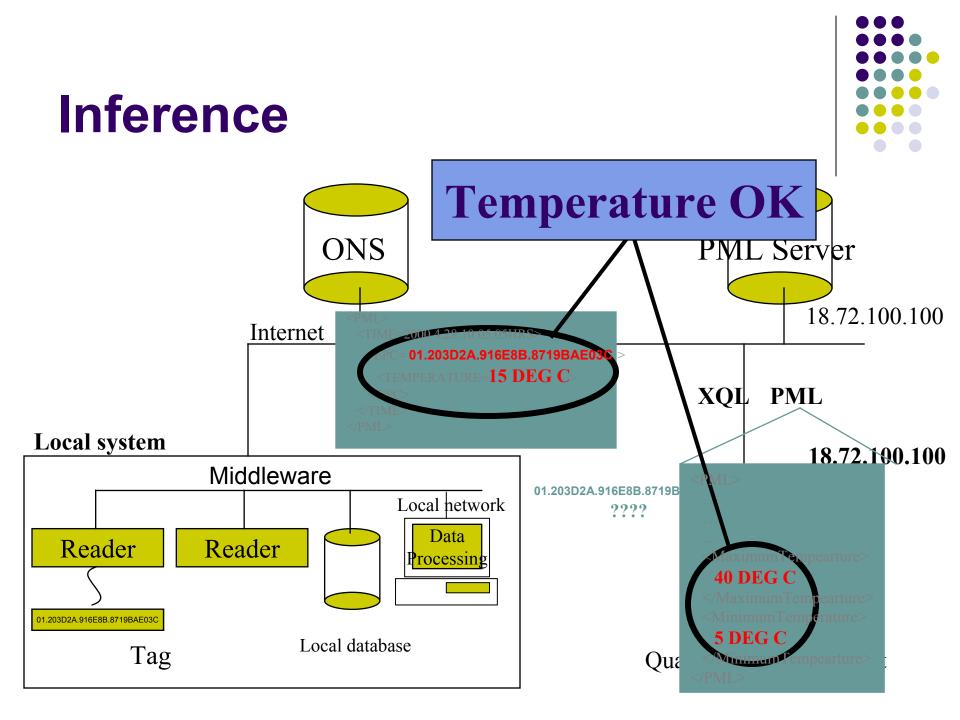




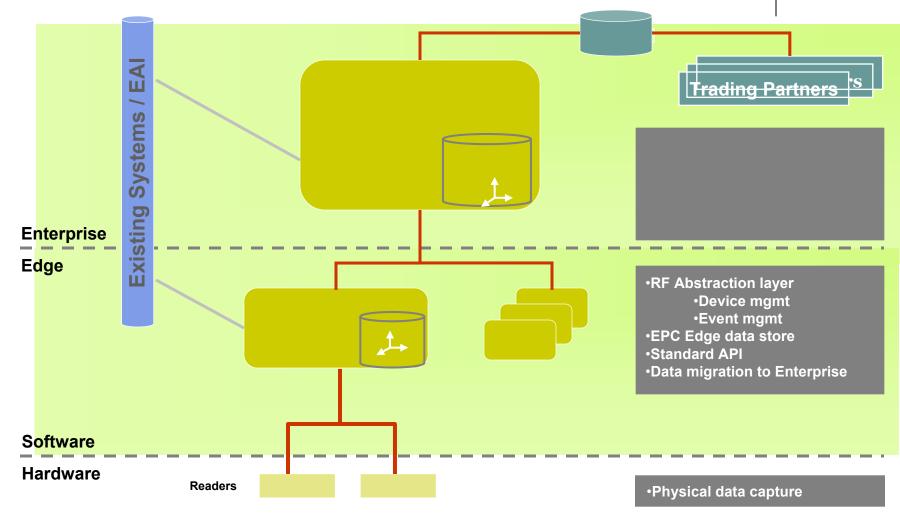
Architecture: Local







Three Layers of an EPC Architecture



Tags

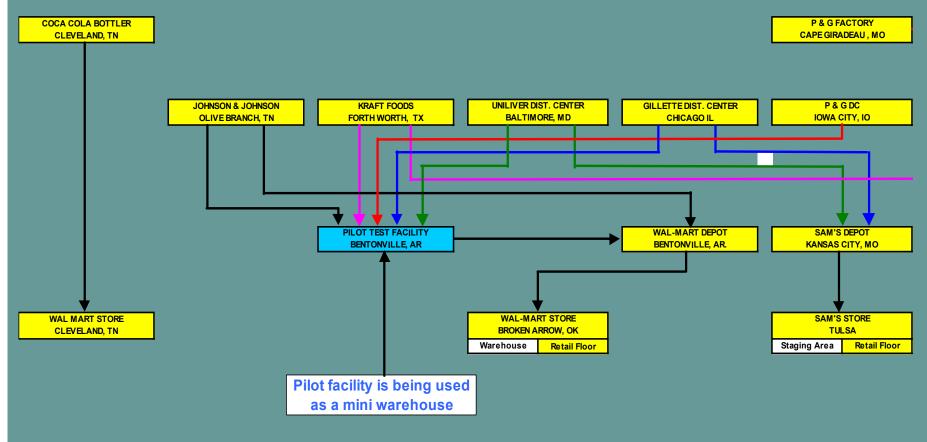
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Field Trial





The Commercialization of EPC



- Landmark Event: EPCglobal is formed
- Many companies have significant tests and pilots underway
- Mandates:
 - DoD
 - Marks & Spencer
 - Tesco
 - Wal-Mart
 - Metro Group
 - Target
 - Albertsons
 - Best Buy
- Other major retailers are continuing to announce their strategies

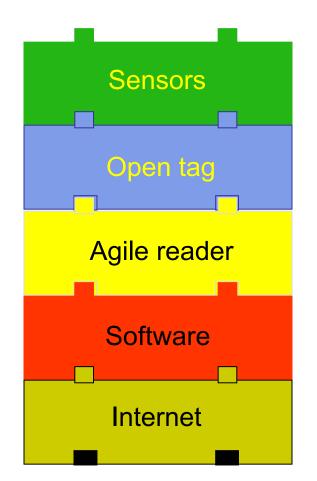
RFID Status

- 3 protocols
 - Class 0 UHF
 - Class I UHF
 - Class I HF
- Tens of manufacturers
 - Tags: Alien, Matrics, Philips, ST Micro, Rafsec,
 - Readers: Alien, Matrics, AWID, ThingMagic, Tyco, Symbol, Samsys,...
- New versions being designed
 - Gen 2 taking off
 - Intermec patent still issue



Key philosophy #1: interoperability





Key philosophy #2: Layers

Class V tags Readers. Can power other Class I, II and III tags; Communicate with Classes IV and V.

Class IV tags: Active tags with broad-band peer-to-peer communication

> Class III tags: semi-passive RFID tags

Class II tags: passive tags with additional functionality

Class 0/Class I: read-only passive tags





Upward compatibility

Vendors

. .



- Chips: Alien, Matrics, Philips, ST Micro
- Readers: Alien, Matrics, Philips, Tagsys, Samsys, ThingMagic, Tyco, Symbol, Markem, AWID
- Software: Sun, Oat Systems, Manhattan, Globe Ranger, Conecterra, SAP, Tibco, Verisign, Vizional,
- Systems: Accenture, PWC/IBM, GEA, ...
- End-Users: Gillette, Wal*Mart, P&G, TESCO, Metro, Target, Wegmans,

Research Issues

- Tag anti-collision
- Reader anti-collision
- Security and privacy
- Advanced sensor networks
- Data routing and handling
- IC Design
- IC manufacturing
 - Silicon processing
 - Chip assembly
- Polymers
- Controls/automation
- Manufacturing systems
- System Synthesis
- Supply chain issues



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Outline, Part II

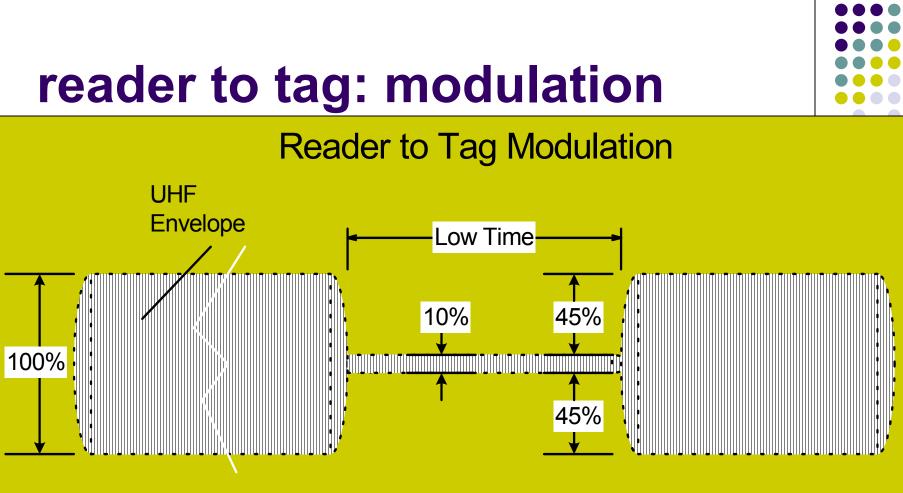
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Components

- Signaling
- Anti-collision
- Functions

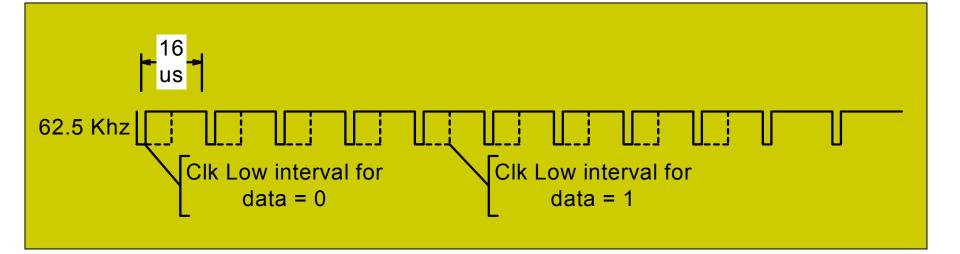




On Off Keying (OOK), Min 90% Modulation Depth

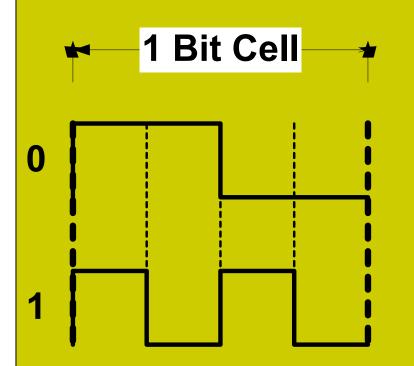


Modulation: reader to tag



tag to reader





- Bit Cell Time: ~8 µs Tag to Reader (128 kbs)
- 2 Transitions = 0
- 4 Transitions = 1
- Always Transitions
 Within a Bit

Anti-collision



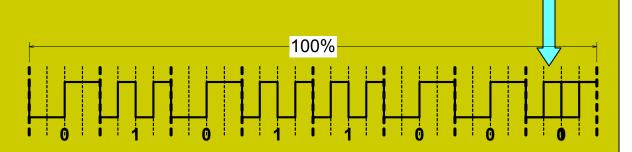
- A Reader Talks First (RTF) System
- Commands Issued from Reader
- Tags Reply at a Later Time While Reader Listens
- Transactions are Self-Contained Operations (Minimal Persistent State Information Required)

Contention Detection



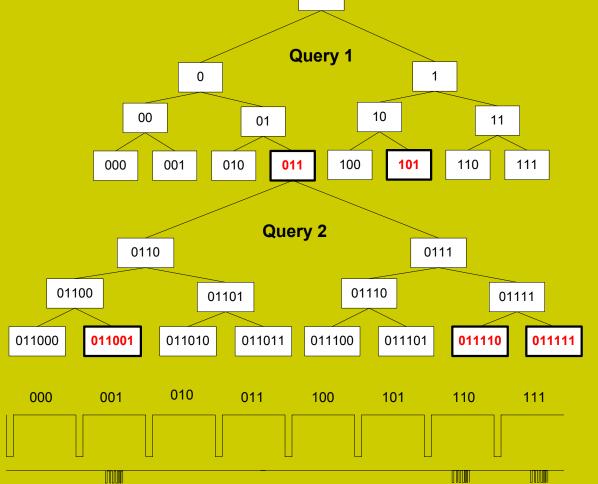
Anti-Collision Algorithm Relies on Detecting Contention (When More than One Tag is Responding to a Reader Command).

Contention- Two Tags, Same Clock Rate, 1-Bit Difference



Anti-Collision





[CMD] = 00001000 (Ping)
[PTR] = 00000000
[LEN] = 00000000 (0)
[VALUE] = 0

```
[CMD] = 00001000 (Ping)
[PTR] = 00000000
[LEN] = 00000011 (3)
[VALUE] = 011
```

Functions

- Write address
- Lock address
- Preload address mask
- Read ID (anti-collision)
- Read payload
- Write payload
- Sleep
- Wake
- Destroy



Outline, Part II

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 - Silicon manufacturing



Does protocol compromise privacy?



Not necessarily. Your choice.

You can destroy the tag and opt out

• or

- You can keep tag for later use
- (physics is your friend)

Mass hijack of tags



- Could happen in <u>destroy</u> or <u>re-programming</u>
- Physics our friend
 - Bandwidth limited: 100's of tags a second anticollision
 - <u>Destroy</u> must be individually addressed
 - So it takes time to kill
 - Surveillance

Issues



- Tags are light-weight
- Anyone can read the tags (promiscuity)
- The same number shows up all the time
- Channel is open and shared



Problem: unique and promiscuous

Kill Serial number?

- Product still readable
- Person can be tracked by constellation

Personalize the number?

- Repeated reads yield same number
- You could still be tracked by constellation





Check out EPCglobal

Public policy

www.epcglobalinc.org/public_policy/ public_policy_guidelines.html

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Outline

- Introduction
- Kinematics
 - In-plane surface motion
 - Out-of-plane motion
- Adhesion and fluid effects
- Experiments
- Conclusions



Introduction



Motivation

- Need methods for handling of small microscopic parts in tag production processes
- A traditional technique to solve scaling problems is parallelization

Topics



Basic kinematics of vibratory part transport

Effects of fluid, and surface/adhesion forces

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Vibration Kinematics

- Want relative motion
- Approaches:
 - Surface micro-features
 - MEMS cilia, rollers, etc.
 - Gas flow nozzle arrays
 - Electrical/magnetic fields
 - Moving Fluid medium flowing over surface
 - Fluidic Self Assembly (FSA Alien Tech's)
 - Vibrating surfaces
 - Time asymmetric in-plane vibrations
 - Out-of-plane vibrations (such as in Bowl Feeders)



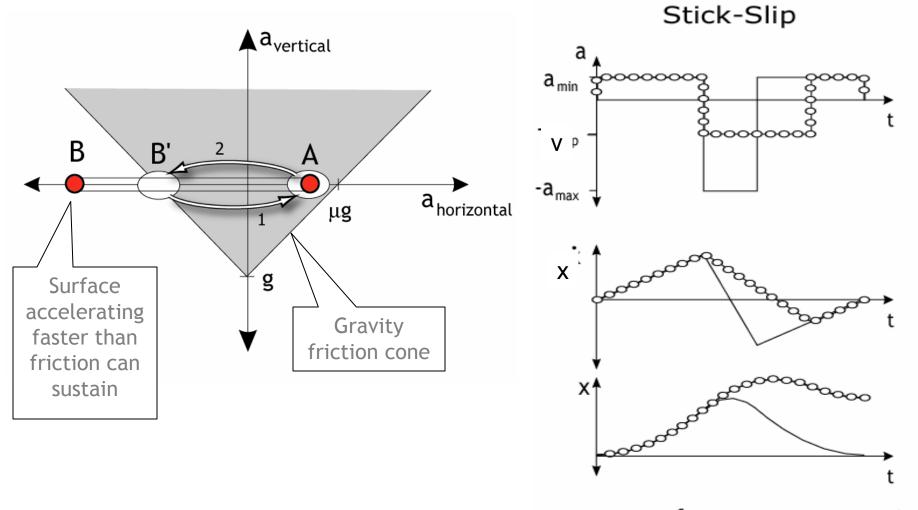
Vibrating Surfaces



In-plane vibrations of a surface if timeasymmetric

- Part moves if surface acceleration is more than friction
- Forward-backward motion?
- Much literature

Example: Stick Slip





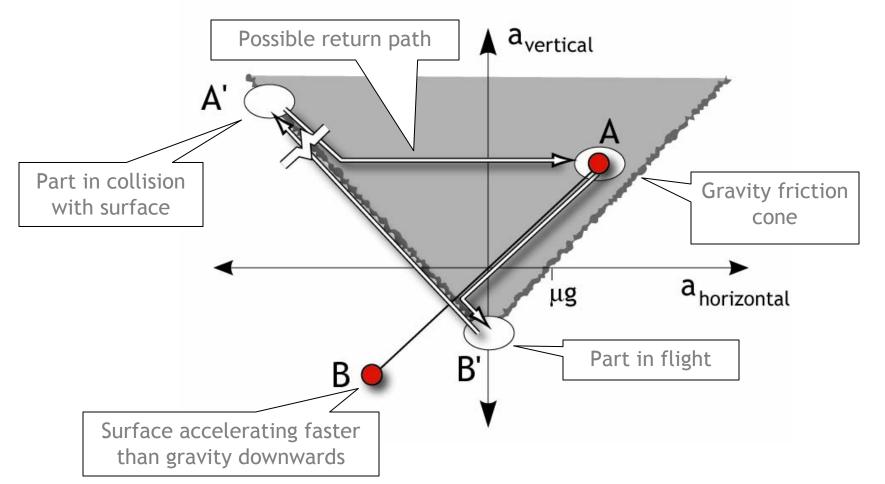
surface 00000 part



Out-of-plane vibrations

- Vertical vibration: extra degree of freedom
- Create hop, move platen back
- Small-scale forces
- Increased accelerations may be needed to compensate

Hopping example





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Adhesion

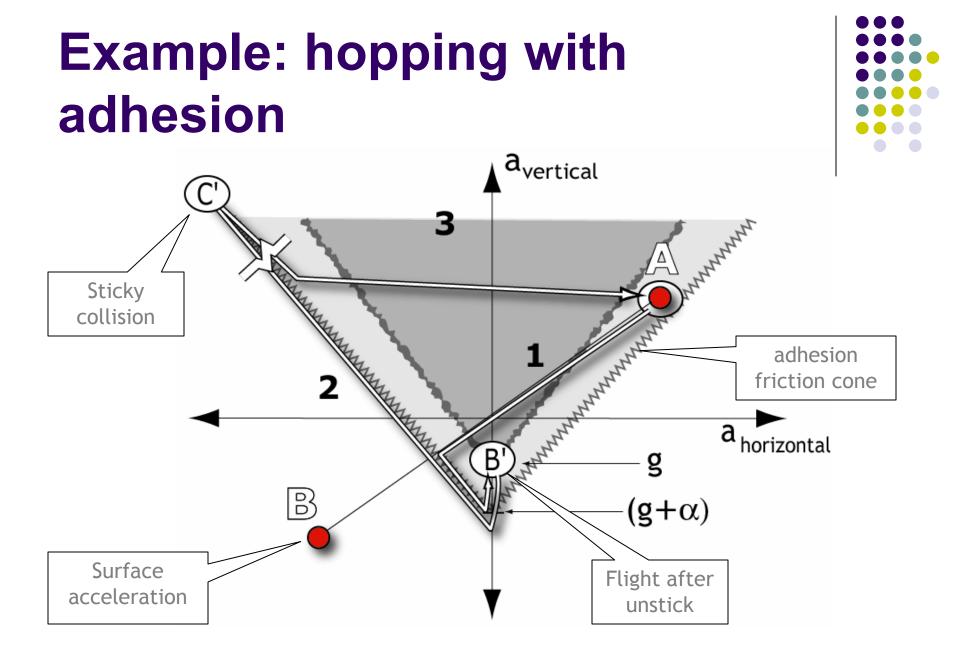


- Adhesion effects become important at small scales
- Van der Waals forces
 - Due to static and quantum mechanically induced dipoles
 - Strong role in inter-molecular and surface phenomena
 - Become important at < 100nm surface separation
 - Adhesion surface energies of ~100mJ/m²
 - Clean atomically smooth surfaces in contact may have adhesion pressures of the order of thousands of atmospheres

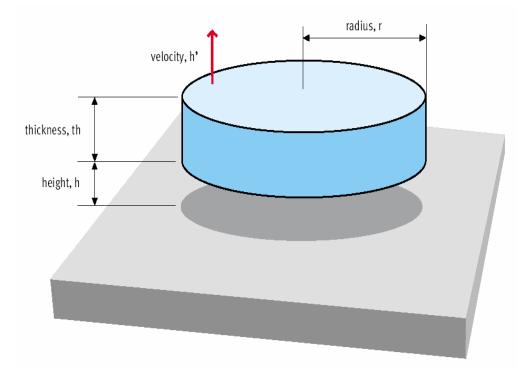
Adhesion effect on vibratory transport



- Larger accelerations are needed
- Too contaminated or too clean are bad
- Can be alleviated by: Roughening or Surfactants
- Strong secondary excitation can "levitate" the parts
 - If done for fractions of the cycle, "creeping" transport can be achieved, where the part moves when vibrations are on and sticks when they are off



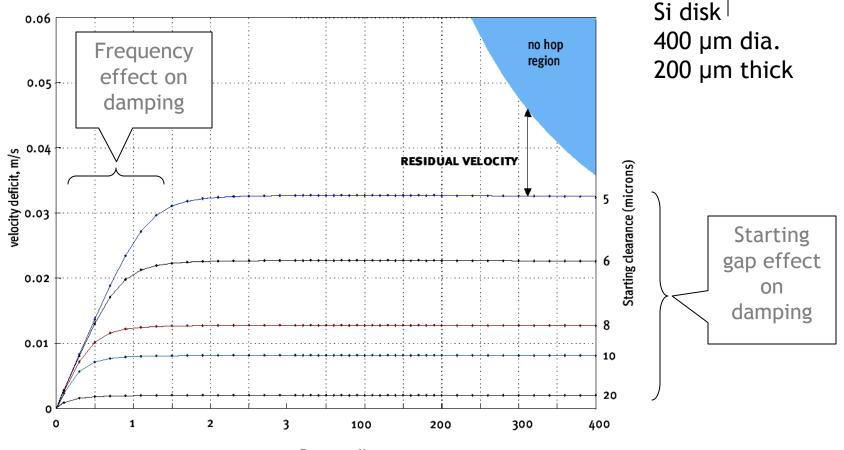
Fluid dynamic scaling



- Sticking due to fluids
- Alleviation
 - use surfaces that are "leaky"
 - Make chip surface bumpy
 - Run in vacuum



velocity loss due to film damping



Frequency, Hz

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Conclusions

- Basic physics
- Ongoing work:
 - Measurements
 - Effects of geometries
 - Test methods
- Design:
 - Chip delivery methods and roll to roll packaging



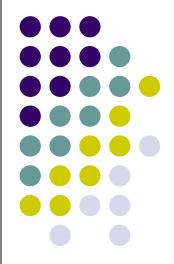
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RFID manufacturing simulation

Gita Swamy Sanjay Sarma



Outline



- Components of an RFID tag
- Understanding the Experiment
- Manufacture
 - Semiconductor
 - Tag
- Results
- Worldwide Fab Capacity

Results

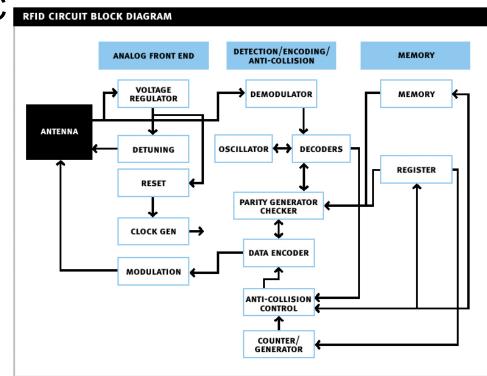
- Total RFID Cost
 - IC + Traditional Assembly: 4.351¢
 IC + Flip Chip Assembly: 3.311¢
- IC Cost: 1.151¢
- Antenna Cost: 11¢
- Assembly: 2.25c ~ 1.15 1¢
- At 10's of billion tags a year



RFID Tag Components



- Antenna
- Mixed-Mode IC
- Packaging



Inputs to model

Process Steps Equipment Benchmark

- Throughput
- Raw material & Utilities
- Labor
- Yield

Overhead

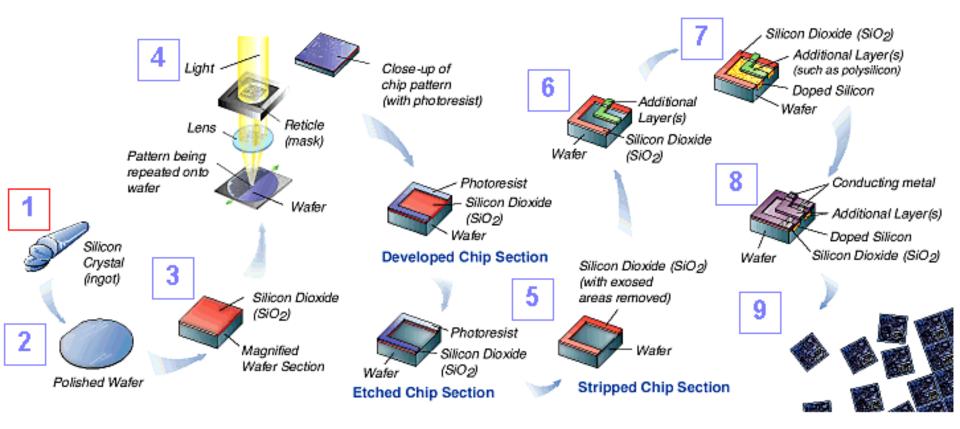
Maintenance

Depreciation





Semiconductor Processing



Process modeling



- R. Leachman, J. Plummer & N. Sato-Misawa, "Understanding fab economics" Competitive Semiconductor Manufacturing, University of California, Berkeley, 1999.
- Leachman & Hodges, "Berkeley Semiconductor Manufacturing" IEEE Transactions on Semiconductor Manufacturing, May 1996.
- J. Bloomsburg, "RFID Tag Manufacturing" MIT UROP, 2002.
- **R. Wright, "Cost Resource Model Detail"** Economic Model Workshop, International Sematech, 2001.

semiconductor process modeling



- Sematech developed benchmark
- 250_A1_82
 Process
 Benchmark
 - 0.25 micron
 - 282 Step
 - 19 Mask
 - 3 Metal
 - 2 Poly

PROCESS DESCRIPTION	TOOL_TYPE
Expose_Implant	Litho_lw
Meas_Overlay	Meas_Overlay
Inspect_PLY	Insp_PLY
Meas_CD	Meas_CD
Implant	Implant_HiE
Implant	Implant_HiE
Implant	Implant_LoE
Plasma_Strip	Dry_Strip(l)
Clean_Post_Strip	Wet_Bench(I)



Driving Variables

- Mask, Metal and Poly Layers
- Wafer starts: 300,000 per year
- 100,000 dies/wafer
- Wafer size: 200mm

	Input	Comment	¥alue					
	Mask Layers		25					
	Metal Layers		3				Create	New Proces
	Poly Layers		2					
	Base calculation number dies	5	50000					
	Number of dies per wafer		114,182					
	Feature Size in mm		1					Clear
	Total cost per wafer		1321.61					
	Total cost per die		0.01157462					
	Worldwide fab capacity		66,560,000					
	Wafer starts		300,000					
	Utilization		0.45%					
		Sensitivity						
	Poly 1							
		Metal						
	\$0.01157462		2	3	- 4	5	6	
lask	7	0.007118275						
	8	0.007235116						
	10	0.00746513						
	15	0.008039686	0.009164546	0.010289017	0.011411	0.012532		
	20	0.008629255	0.009748212	0.010873598	0.011991	0.013123	0.014244	
	25	0.009209519	0.010328784	0.011453179	0.012579	0.013702	0.01482	



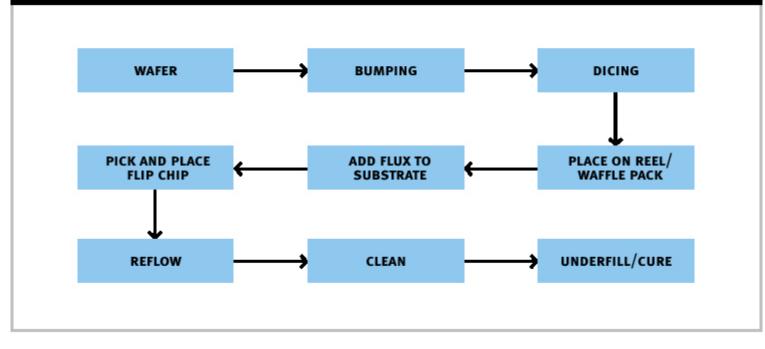
Assembly Process

- Assembly Process Steps
 - Thinning
 - Dicing
 - Assembly
 - Traditional
 - Flip Chip
 - Fluidic Self Assembly
 - Vibratory Assembly
 - Tag Test

Flip chip



FLIP CHIP ASSEMBLY PROCESS STEPS





Assembly Process

• Types of Runs

Unit Machine

Line Maximized

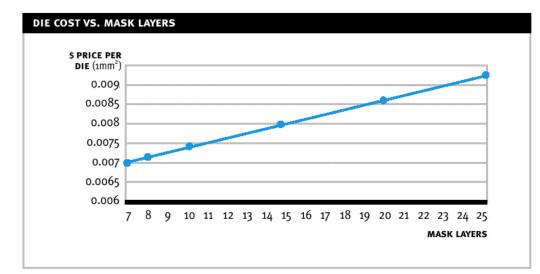
Process	Throughtpu Unit/Hr	Pipeline Tpul Die/Hr	Used Tput Die/Hr	Utilizatio Hr/Day		Yield %	Wattage KW	Floor space Sq Ft	Machine Cost \$	Maintainence cost \$/Yr	Total Cost \$/Yr
Thinning	10	1130400	1130400	16	5	97%	20	100	\$425,000	\$5,000	\$101,923.4
Dicing	6	678240	678240	16	5	97%	20	21	\$300,000	\$5,000	\$72,164.0
Traditional Assembly	3750	3750	NA	16	5	97%	20	200	\$935.000	\$5.000	\$216.983.4
Traditional Assembly Flip Chip Assembly	3750	3750	12/12/12/20	10000		97% 98%		10.9425	\$935,000 \$1,200,000		\$216,983.4 \$273,853.4

Results

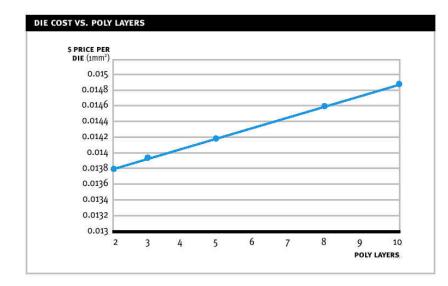
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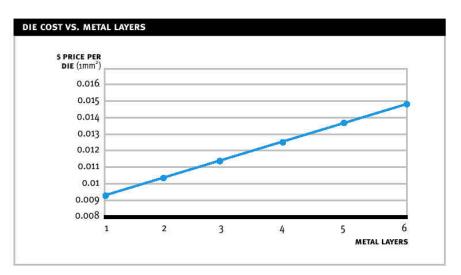


Results: Die Cost



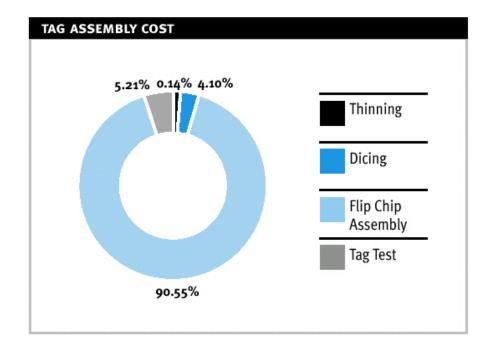


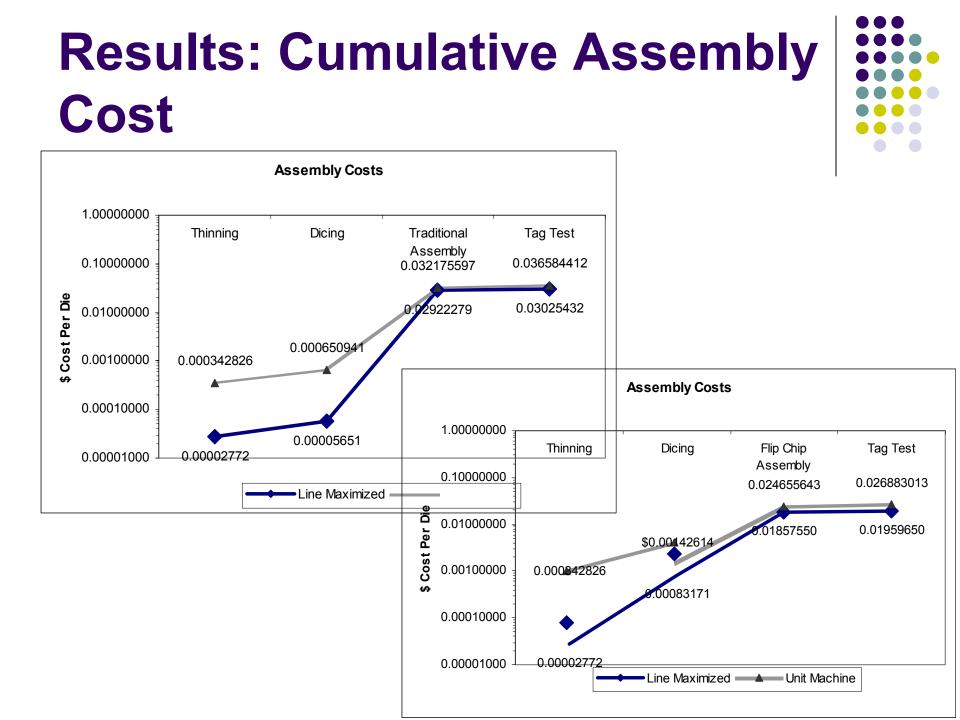




Results: Assembly Cost Breakdown

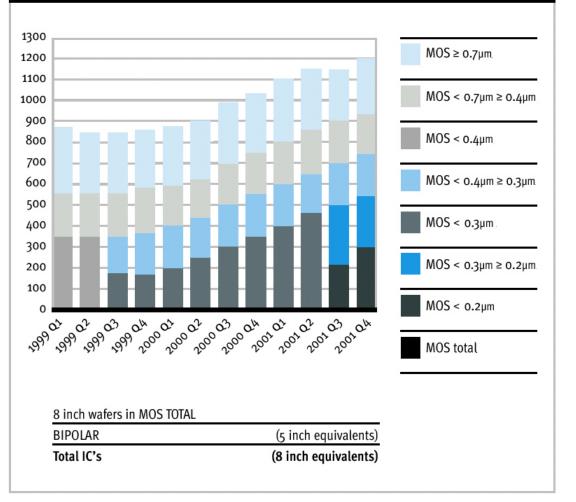






Worldwide Fab Capacity

IC WAFER – FAB CAPACITY IN WAFER STARTS PER WEEK X 1000



- Assume 1 billion tags a day
- 100,000 dies/wafer
- 20% of world silicon capacity
- Fabs 15% idle today



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Conclusions

