CHAPTER XI

BASIC APPLICATIONS

11.1 INTRODUCTION

The operational amplifier is an extremely versatile general-purpose linear circuit. Clearly a primary reason for studying this device is to determine how it can best be used to solve design problems. Since this book is intended as a text book and not as a handbook, we hope to accomplish our objective by giving the reader a thorough understanding of the behavior of the operational amplifier so that he can innovate his own applications, rather than by giving him a long list of connections that others have found useful. Furthermore, there are a number of excellent references[1] available that provide extensive collections of operational-amplifier circuits, and there is little to be gained by competing with these references for completeness.

We have already seen several operational-amplifier connections in the examples used in preceding sections. In this and the following chapter we shall extend our list of applications in order to illustrate useful basic techniques. We hope that the reader finds these topologies interesting, and that they help provide the concepts necessary for imaginative, original design efforts. Some of the common hazards associated with the use of operational amplifier are discussed, as is the measurement and specification of performance characteristics. The vitally important issue of amplifier compensation for specific applications is reserved for Chapter 13.

11.2 SPECIFICATIONS

A firm understanding of some of the specifications used to describe operational amplifiers is necessary to determine if an amplifier will be satisfactory in an intended application. Unfortunately, completely specifying a

[1] A few of these references are: Philbrick Researches, Inc., *Applications Manual of Computing Amplifiers.* G. A. Korn and T. M. Korn, *Electronic Analog and Hybrid Computers*, 2nd Edition, McGraw-Hill, New York, 1972. J. G. Graeme, G. E. Tobey, and L. P. Huelsman (Editors), *Operational Amplifiers, Design and Applications*, McGraw-Hill, New York, 1971. Analog Devices, Inc., *Product Guide*, 1973. National Semiconductor Corporation, *Linear Applications Handbook*, 1972.

complex circuit is a virtually impossible task. The problem is compounded by the fact that not all manufacturers specify the same quantities, and not all are equally conservative with their definitions of "typical," "maximum," and "minimum." As a result, the question of greatest interest to the designer (will it work in my circuit?) is often unanswered.

11.2.1 Definitions

Some of the more common specifications and their generally accepted definitions are listed below. Since there are a number of available operational amplifiers that are not intended for differential operation (e.g., amplifiers that use feedforward compensation are normally single-input amplifiers), the differences in specifications between differential- and single-input amplifiers are indicated when applicable.

Input offset voltage. The voltage that must be applied between inputs of a differential-input amplifier, or between the input and ground of a single-input amplifier, to make the output voltage zero. This quantity may be specified over a given temperature range, or its incremental change (drift) as a function of temperature, time, supply voltage, or some other parameter may be given.

Input bias current. The current required at the input of a single-input amplifier, or the average of the two input currents for a differential-input amplifier.

Input offset current. The difference between the two input currents of a differential-input amplifier. Both offset and bias current are defined for zero output voltage, but in practice the dependence of these quantities on output voltage level is minimal. The dependence of these quantities on temperature or other operating conditions is often specified.

Common-mode rejection ratio. The ratio of differential gain to common-mode gain.

Supply-voltage sensitivity. The change in input offset voltage per unit change in power-supply voltage. The reciprocal of this quantity is called the supply-voltage rejection ratio.

Input common-mode range. The common-mode input signal range for which a differential amplifier remains linear.

Input differential range. The maximum differential signal that can be applied without destroying the amplifier.

Output voltage range. The maximum output signal that can be obtained without significant distortion. This quantity is usually specified for a given load resistance.

Input resistance. Incremental quantities are normally specified for both differential (between inputs) and common-mode (either input to ground) signals.

Output resistance. Incremental quantity measured without feedback unless otherwise specified.

Voltage gain or open-loop gain. The ratio of the change in amplifier output voltage to its change in input voltage when the amplifier is in its linear region and when the input signal varies extremely slowly. This quantity is frequently specified for a large change in output voltage level.

Slew rate. The maximum time rate of change of output voltage. This quantity depends on compensation for an externally compensated amplifier. Alternatively, the maximum frequency at which an undistorted given amplitude sinusoidal output can be obtained may be specified.

Bandwidth specifications. The most complete specification is a Bode plot, but unfortunately one is not always given. Other frequently specified quantities include unity-gain frequency, rise time for a step input or half-power frequency for a given feedback connection. Most confusing is a gain-bandwidth product specification, which may be the unity-gain frequency, or may be the product of closed-loop voltage gain and half-power bandwidth in some feedback connection.

Even when operational-amplifier specifications are supplied honestly and in reasonable detail, the prediction of the performance of an amplifier in a particular connection can be an involved process. As an example of this type of calculation, consider the relatively simple problem of finding the output voltage of the noninverting amplifier connection shown in Fig. 11.1 when $v_I = 0$. The voltage offset of the amplifier is equal to E_O. It is assumed that the low-frequency voltage gain of the amplifier a_0 is very large so that the voltage between the input terminals of the amplifier is nearly equal to E_O. (Recall that with E_O applied to the input terminals, $v_O = 0$. If a_0 is very large, any other d-c output voltage within the linear region of the

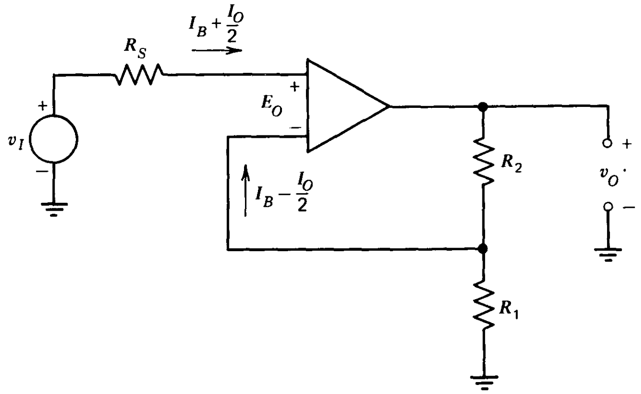


Figure 11.1 Noninverting amplifier.

amplifier can be obtained with a voltage of approximately E_O applied between inputs.) The currents at the amplifier input terminals expressed in terms of the bias current I_B and the offset current I_O are also shown in this figure.[2]

The voltage and current values shown in the figure imply that, for $v_I = 0$,

$$-R_S\left(I_B + \frac{I_O}{2}\right) - v_O\left(\frac{R_1}{R_1 + R_2}\right) + \left(I_B - \frac{I_O}{2}\right)\frac{R_1R_2}{R_1 + R_2} = E_O \quad (11.1)$$

Solving for v_O yields

$$v_O = -\frac{(R_2 + R_1)}{R_1}E_O - \left(\frac{R_1 + R_2}{R_1}\right)R_S\left(I_B + \frac{I_O}{2}\right) + R_2\left(I_B - \frac{I_O}{2}\right) \quad (11.2)$$

This equation shows that the output voltage attributable to amplifier input current can be reduced by scaling resistance levels, but that the error resulting from voltage offset is irreducible since the ratio $(R_1 + R_2)/R_1$ presumably must be selected on the basis of the required ideal closed-loop gain. Equation 11.2 also demonstrates the well-known result that balancing the resistances connected to the two inputs eliminates offsets attributable to input bias current, since with $R_1R_2/(R_1 + R_2) = R_S$, the output voltage is independent of I_B.

As another example of the use of amplifier specifications, consider a device with an offset E_O, a d-c gain of a_0, and a maximum output voltage V_{OM}. The maximum differential input voltage required in order to obtain any static output voltage within the dynamic range of the amplifier is then[3]

$$V_{IM} = E_O + \frac{V_{OM}}{a_0} \quad (11.3)$$

This equation shows that values of a_0 in excess of V_{OM}/E_O reduce the amplifier input voltage (which must be low for the closed-loop gain to approximate its ideal value) only slightly. We conclude that if $a_0 > V_{OM}/E_O$, further operational-amplifier design efforts are better devoted to lowering offset rather than to increasing a_0.

[2] The specification of the input currents in terms of bias and offset current does not, of course, indicate which input-terminal current is larger for a particular amplifier. It has been arbitrarily assumed in Fig. 11.1 that the offset current adds to the bias current at the noninverting input and subtracts from it at the inverting input.

[3] The quantities in the equation are assumed to be maximum magnitudes. The possibility of cancellation because of algebraic signs exists for only one polarity of output voltage, and is thus ignored when calculating the maximum magnitude of the input voltage.

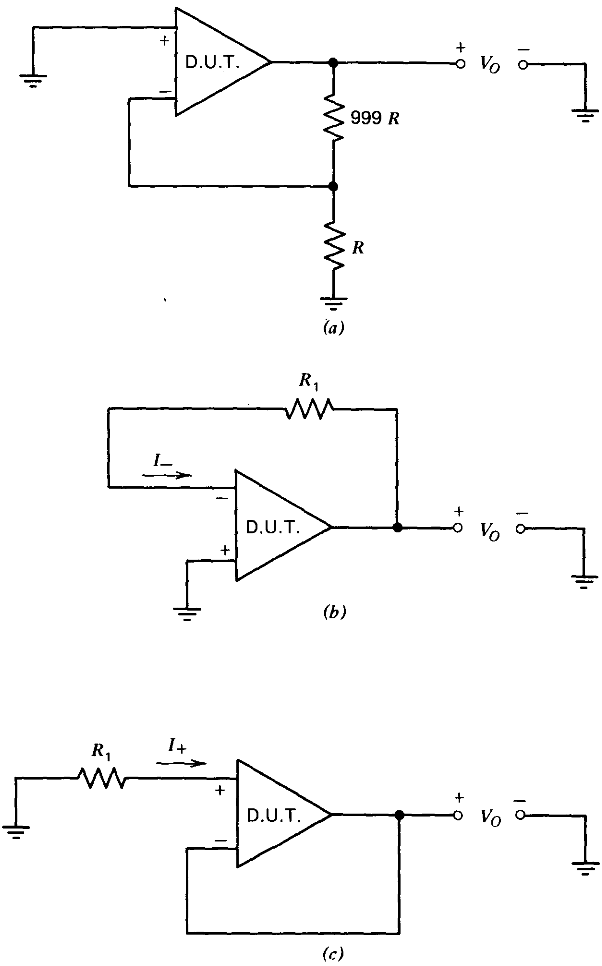


Figure 11.2 Circuits used to determine offset voltage and input currents. D.U.T. = Device Under Test. (*a*) Measurement of offset voltage. (*b*) Measurement of I_-. (*c*) Measurement of I_+.

11.2.2 Parameter Measurement

One way to bypass the conspiracy of silence that often surrounds amplifier specifications is to measure the parameters that are important in a particular application. Measurement allows the user to determine for himself how a particular manufacturer defines "typical," "maximum," and "minimum," and also permits him to grade circuits so that superior units can be used in the more demanding applications.

The d-c characteristics exclusive of open-loop gain are relatively straightforward to measure. Circuits that can be used to measure the input offset voltage E_O and the input currents at the two input terminals, I_+ and I_-, are shown in Fig. 11.2. In the circuit of Fig. 11.2*a*, assume that resistor values are chosen so that $|E_O| \gg |I_-R|$. The quiescent voltages are

$$(-10^{-3}V_O + E_O)a_0 = V_O \tag{11.4}$$

for an appropriately chosen reference polarity for E_O. Solving this equation for V_O yields

$$V_O = \frac{a_0 E_O}{1 + 10^{-3}a_0} \simeq 10^3 E_O \tag{11.5}$$

Thus we see that this circuit uses the amplifier to raise its own offset voltage to an easily measured level.

If the resistor R_1 in Figs. 11.2*b* and 11.2*c* is chosen so that both $|I_-R_1|$ and $|I_+R_1| \gg |E_O|$, the output voltages are

$$V_O = I_-R_1 \tag{11.6}$$

and

$$V_O = -I_+R_1 \tag{11.7}$$

respectively. The measurement of I_- and I_+ allows direct calculation of offset and bias currents, since we recall from earlier definitions that the bias current is equal to the average of I_+ and I_-, while the offset current is equal to the magnitude of the difference between these two quantities.

A test box that includes a socket for the device under test and incorporates mode switching to select among the tests is easily constructed. Results can be displayed on an inexpensive D'Arsonval meter movement, since resistor values can be chosen to yield output voltages on the order of one volt. The low-pass characteristics of the meter movement provides a degree of noise rejection that improves the accuracy of the measurements. If further noise filtering is required, moderate-value capacitors may be used in parallel with resistors 999R and R_1 in Fig. 11.2.

The offset measurement circuit shown in Fig. 11.2*a* requires large loop-transmission magnitude for proper operation. If there is the possibility that the low-frequency loop transmission of a particular amplifier is too small, the alternative circuit shown in Fig. 11.3 can be used to measure offset. The second amplifier provides very large d-c gain with the result that the voltage out of the amplifier under test is negligible. At moderate frequencies, the second amplifier functions as a unity-gain inverter so that loop stability is not compromised by the integrator characteristics that result if the feedback resistor R is eliminated. Lowering the value of this

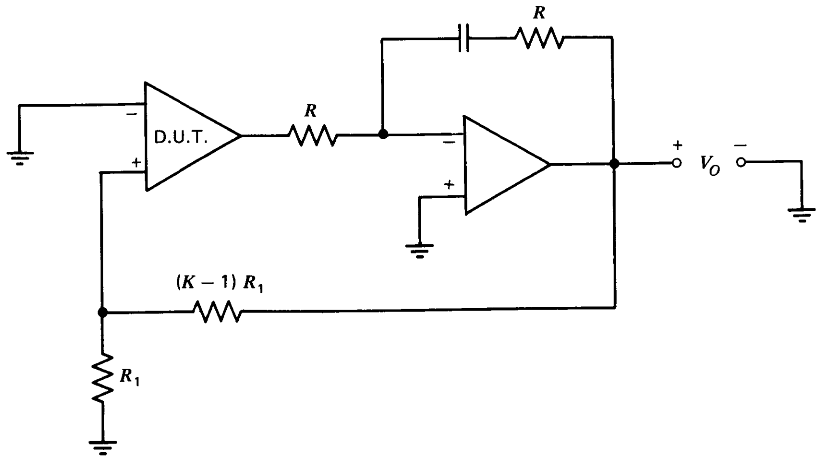


Figure 11.3 Offset-measurement circuit with increased loop transmission.

feedback resistor relative to the input resistor of the second amplifier may improve stability, particularly when the $(K - 1)R_1$ resistor is bypassed for noise reduction. Since this connection keeps the output voltage from the amplifier under test near ground, V_O will be (in the absence of input-current effects) simply equal to KE_O.

The supply-voltage rejection ratio of an amplifier can be measured with the same circuitry used to measure offset if provision is included to vary voltages applied to the amplifier. The supply-voltage rejection ratio is defined as the ratio of a change in supply voltage to the resulting change in input offset voltage.

The technique of including a second amplifier to increase loop transmission simplifies the measurement of common-mode rejection ratio (see Fig. 11.4). If the differential gain a_0 of the amplifier is large compared to its common-mode gain a_{cm}, we can write

$$0 = a_{cm}v_{CM} + \frac{a_0 v_A}{K} \tag{11.8}$$

Thus

$$\left|\frac{a_0}{a_{cm}}\right| = \text{CMRR} = \left|\frac{Kv_{CM}}{v_A}\right| \tag{11.9}$$

Since the voltage v_A also includes a component proportional to the offset voltage of the amplifier, it may be necessary to use incremental measurements to determine accurately rejection ratio.

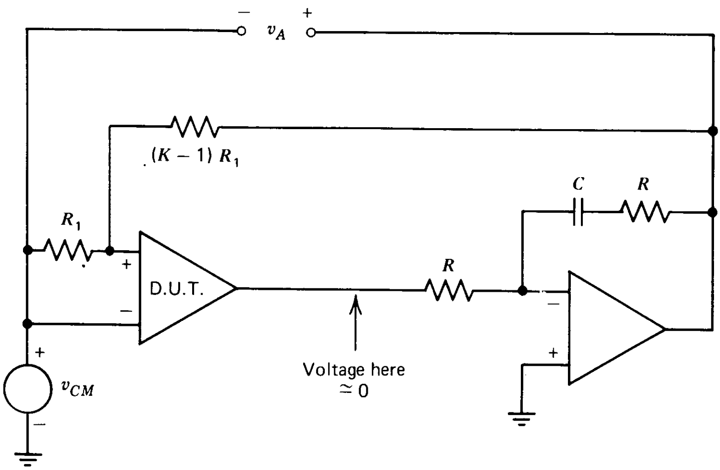


Figure 11.4 Circuit for measuring common-mode rejection ratio.

The slew rate of an amplifier may be dependent on the time rate of change of input-signal common-mode level and will be a function of compensation for an amplifier with selectable compensation. Standardized results that allow intercomparison of various amplifiers can be obtained by connecting the amplifier as a unity-gain inverter and applying a step input that sweeps the amplifier output through most of its dynamic range. Diode clamping at the inverting input of the amplifier can be used to prevent large common-mode signals. (See Section 13.3.7 for a representative circuit.) Alternatively, the maximum slew rate in a specific connection of interest can often be determined by applying a large enough input signal to force the maximum time rate of change of amplifier output voltage.

The open-loop transfer function of an amplifier is considerably more challenging to measure. Consider, for example, the problem of determining d-c gain. We might naively assume that the amplifier could be operated open loop (after all, we are measuring open-loop gain), biased in its linear region by applying an appropriate input quiescent level, and gain determined by adding an incremental step at the input and measuring the change in output level. The hazards of this approach are legion. The output signal is normally corrupted by noise and drift so that changes are difficult to determine accurately. We may also find that the amplifier exhibits bistable behavior, and that it is not possible to find a value for input voltage that forces the amplifier output into its linear region. This phenomenon results from positive thermal feedback in an integrated circuit, and can also occur in discrete designs because of self-heating, feedback through shared bias networks or power supplies, or for other reasons. The positive feedback that leads to this behavior is swamped by negative feedback applied around the amplifier in normal applications, and thus does not disturb performance in the usual connections.

After some frustration it is usually concluded that better results may be obtained by operating the amplifier in a closed-loop connection. Signal amplitudes can be adjusted for the largest output that insures linear performance at some frequency, and the corresponding input signal measured. The magnitude and angle of the transfer function can be obtained if the input signal can be accurately determined. Unfortunately, the signal at the amplifier input is usually noisy, particularly at frequencies where the open-loop gain magnitude is large. A wave analyzer or an amplifier followed by a phase-sensitive demodulator driven at the input frequency may be necessary for accurate measurements. This technique can even be used to determine a_0 if the amplifier is compensated so that the first pole in its open-loop transfer function is located within the frequency range of the detector.

There are also indirect methods that can be used to approximate the open-loop transfer function of the amplifier. The small-signal closed-loop frequency or transient response can be measured for a number of different values of frequency-independent feedback f_0. A Nichols chart or the curves of Fig. 4.26 may then be used to determine important characteristics of $a(j\omega)$ at frequencies near that for which $|a(j\omega)f_0| = 1$. Since various values of f_0 are used, $a(j\omega)$ can be determined at several different frequencies. This type of measurement often yields sufficient information for use in stability calculations.

A third possibility is to test the amplifier in a connection that provides a multiple of the signal at the amplifier input, in much the same way as does the circuit suggested earlier for offset measurement. Figure 11.5 shows one

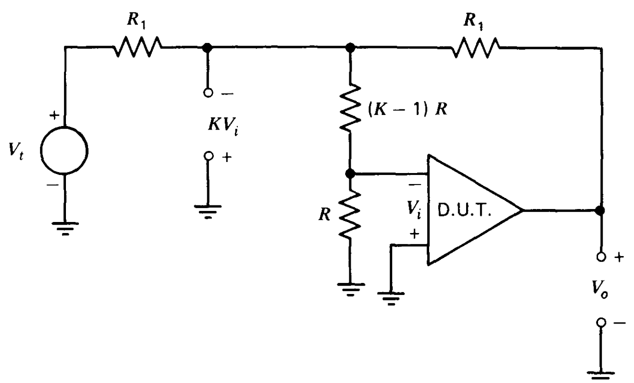


Figure 11.5 Connection for measuring the open-loop transfer function.

possibility. The signal at the junction of the two resistors labeled R_1 is K times as large as the input signal applied to the amplifier, and can be compared with either V_o or V_t (which is equal to $-V_o$ when the loop transmission is large) in order to determine the open-loop transfer function of the amplifier. Note that if the signal at the junction of the two equal-value resistors is compared with V_o, this method does not depend on large loop transmission.

While this method does scale the input signal, it does not provide filtering, with the result that some additional signal processing may be necessary to improve signal-to-noise ratio.

11.3 GENERAL PRECAUTIONS

The operational amplifier is a complex circuit that is used in a wide variety of connections. Frequently encountered problems include amplifier destruction because of excessive voltages or power dissipation and oscillation. The precautions necessary to avoid these hazards depend on the specific operational amplifier being used. We generally find, for example, that discrete-component amplifiers are more tolerant of abuse than are integrated-circuit units, since more sophisticated protective features are frequently included in discrete designs.

This section indicates some of the more common problem areas and suggests techniques that can be used to avoid them.

11.3.1 Destructive Processes

Excessive power-supply voltages are a frequent cause of amplifier damage. Isolation from uncertain supply-voltage levels via a resistor-Zener diode combination, as shown in Fig. 11.6, is one way to eliminate this hazard. The Zener diodes also conduct in the forward direction in the event of supply-voltage reversal. A better solution in systems that include a large number of operational amplifiers is to make sure that the power supplies include "crowbar"-type protection that limits voltages to safe levels in the event of power-supply failure.

Excessive differential input voltage applied to an operational amplifier may damage the input-transistor pair. If input voltages in excess of about 0.6 volt are applied to a normal differential-amplifier connection, the base-to-emitter junction of one of the members of the pair will be reverse biased. Further increases in applied differential voltage eventually result in reverse breakdown.

The base-to-emitter junction can be burned out if sufficient power is applied to it. A more subtle problem, however, is that base-to-emitter re-

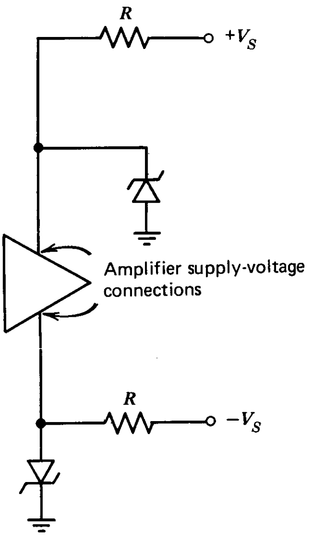


Figure 11.6 Supply-voltage limiting.

verse breakdown, even at low power levels, often irreversibly lowers the current gain of bipolar transistors. Thus the input current of an amplifier can be permanently increased by this mechanism. The potential for low power level base-to-emitter breakdown exists in many connections. Consider, for example, the usual integrator connection. If amplifier power is shut off with the feedback capacitor charged, the differential input voltage limit may be exceeded.

One practical solution is to include a pair of clamp diodes between the input terminals of the amplifier. Since the voltage between these terminals is nearly zero under normal operating conditions, the diodes have no effect until excessive voltage levels are reached.

Excessive power dissipation can result in some designs if the output terminal is shorted to ground. This possibility exists primarily in early integrated-circuit designs that do not include current-limiting circuits. More modern integrated-circuit designs, as well as most discrete circuits, are protected for output-to-ground shorts at normal supply-voltage levels and room-temperature operation. Some of these amplifiers are not protected for output shorts to either supply voltage, or output-to-ground shorts at elevated temperatures.

The compensation or balance terminals of operational amplifiers are frequently connected to critical low-level points, and any signal applied to these terminals invites disaster. The author is particularly adept at demonstrating this mode of destruction by shorting adjacent pins to each other or a pin to ground with an oscilloscope probe.

11.3.2 Oscillation

One of the most frequent complaints about operational amplifiers is that they oscillate in connections that the user feels should be stable. This phenomenon usually reflects a problem with the user rather than with the amplifier, and most of these instabilities can be corrected by proper design practice.

One frequent reason for oscillation is that dynamics associated with the load applied to the amplifier or the feedback network connected around it combine with the open-loop transfer function of the amplifier to produce feedback instabilities. The material presented in the chapters on feedback provides the general guidelines to eliminate these types of oscillations. Specific examples are given in Chapter 13.

Another common cause of oscillation is excessive power-connection impedance. This problem is particularly severe with high-frequency amplifiers because of the inductance of the leads that couple the power supply to the amplifier. In order to minimize difficulties, it is essential to properly decouple or bypass all power-supply leads to amplifiers without internal decoupling networks. Good design practice includes using a fairly large value (>1 μF) solid-tantalum electrolytic capacitor from the positive and the negative power supply to ground on each circuit board. Individual amplifiers should have ceramic capacitors (0.01 μF to 0.1 μF) connected directly from their supply terminals to a common ground point. The single ground connection between the two decoupling capacitors should also serve as the tie point for the input-signal common, if possible. Lead length on both the supply voltage and the ground side of these capacitors is critical since series inductance negates their value. Ground planes may be mandatory in high-frequency circuits for acceptably low ground-lead inductance. If low supply currents are anticipated, crosstalk between amplifiers can be reduced by including small ($\simeq 22\ \Omega$) series resistors in each decoupling network, as shown in Fig. 11.7.

In addition to reducing supply-line impedance, decoupling networks often lower the amplitude of any supply-voltage transients. Such transients are particularly troublesome with amplifiers that use capacitive minor-loop feedback for compensation, since the feedback element can couple transients applied to a supply-voltage terminal directly to the amplifier output.

The open-loop transfer function of many operational amplifiers is dependent on the impedance connected to the noninverting input of the amplifier. In particular, if a large resistor is connected in series with this terminal

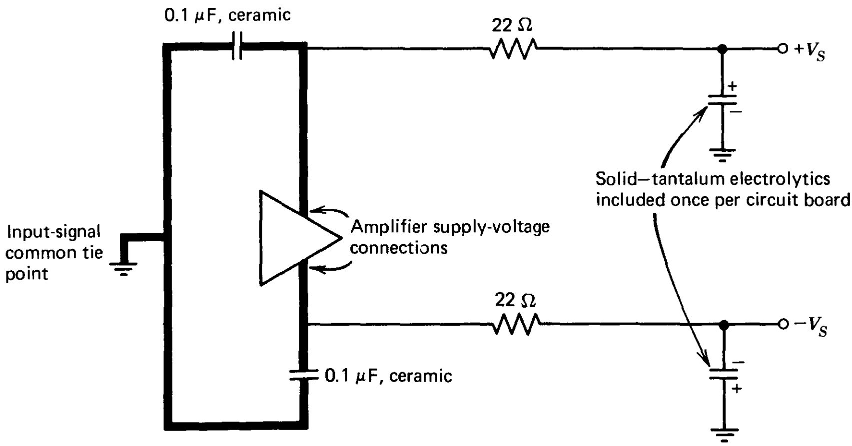


Figure 11.7 Power-supply decoupling network. *Note.* Heavy leads must be short.

(possibly to balance resistances seen at both inputs, thus reducing effects of bias currents), the bandwidth of the amplifier may deteriorate, leading to oscillation. In these cases a capacitor should be used to shunt the non-inverting input of the amplifier to the common input-signal and power-supply-decoupling ground point.

The input capacitance of an operational amplifier may combine with the feedback network to introduce a pole that compromises stability. Figure 11.8 is used to illustrate this problem. It is assumed that the input conductance of the amplifier is negligibly small, and that its input capacitance is modeled by the capacitor C_i shown in Fig. 11.8. If the capacitors shown with dotted connections in this figure are not present, the loop transmis-

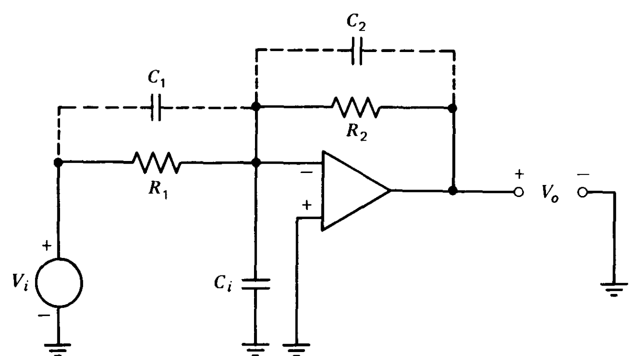


Figure 11.8 Effect of input capacitance.

sion includes a term $1/[(R_1 \| R_2)C_i s + 1]$. If capacitor C_2 is included and values are chosen so that $R_2C_2 = R_1C_i$, the transfer function of the feedback network from the amplifier output to its inverting input becomes frequency independent. In practice, it is not necessary to match time constants precisely. A minor mismatch introduces a closely spaced pole-zero doublet, which normally has little effect on stability, into the loop-transmission expression.

A possible difficulty is that the inclusion of capacitor C_2 changes the ideal closed-loop gain of the amplifier to

$$\frac{V_o(s)}{V_i(s)} = -\frac{R_2}{R_1(R_2C_2s + 1)} \tag{11.10}$$

An alternative is to include both capacitors C_1 and C_2. If $R_1C_1 = R_2C_2$ and $C_1 + C_2 \gg C_i$, the ideal closed-loop gain maintains its original value

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \tag{11.11}$$

while the feedback-network transfer function from the output to the inverting input of the operational amplifier becomes essentially frequency independent.

11.3.3 Grounding Problems

Improper grounding is a frequent cause of poor amplifier performance. While a detailed study of this subject is beyond the scope of this book, some discussion is in order.

One frequent grounding problem stems from voltage drops in ground lines as a consequence of current flow through these lines. Figure 11.9 illustrates an obviously poor configuration. Here both a signal source and a power supply are connected to a single ground point. However, the current through a load is returned to the low side of the power supply via a wire that also sets the potential at the noninverting input of the operational amplifier. If this current creates a potential V_g at the noninverting input with respect to system ground, the amplifier output voltage with respect to system ground will be

$$V_o = -\frac{R_2}{R_1}V_i + \frac{R_1 + R_2}{R_1}V_g \tag{11.12}$$

The error term involving current flow through the ground return line can be substantial, since narrow printed-circuit conductors and connector pins can have considerable resistance and inductance.

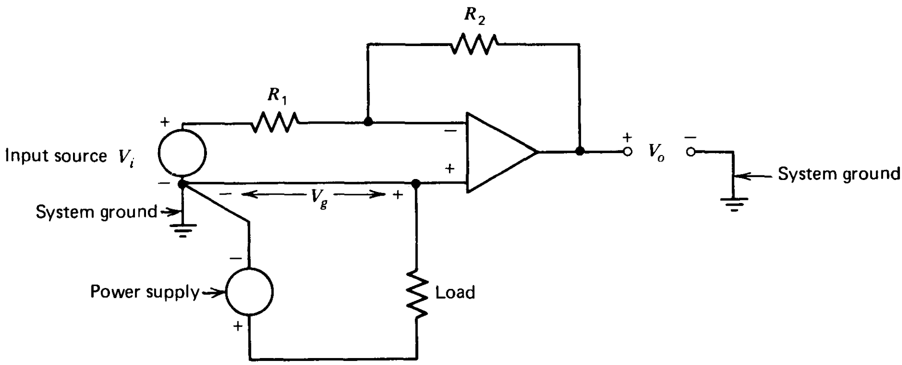


Figure 11.9 An example of poor grounding technique.

While the obvious topology illustrated in Fig. 11.9 is relatively easy to avoid, somewhat better disguised variations occur with disturbing frequency. The solution is to design the system with two different ground networks. One of these networks, called *signal ground*, serves as the return for critical points such as signal sources, feedback networks, and precision voltage references. Every attempt is made to keep both a-c and d-c currents in this network small so that it is essentially an equipotential network. High currents from noncritical loads (an excellent example is the logic often found in complex systems that include both analog and digital components) have their own ground-return network called *power ground.* These two grounds connect at *only one* point, which is also the low side of all system power supplies.

11.3.4 Selection of Passive Components

The passive components used in conjunction with operational amplifiers must be selected with care to obtain satisfactory performance.

Metal-film or carbon-film resistors with tolerances of 1% are inexpensive and readily available. These resistors can be obtained with temperature coefficients as low as 25 parts per million per degree Centigrade, and have fair long-term stability. They are acceptable in less demanding applications. We should note, however, that if 1% resistors are used, loop transmissions in excess of 100 are wasted in many connections.

Wire-wound resistors may be used where accuracy, stability, and temperature coefficient are of primary concern, since units are available that can maintain values to within 0.01% or better with time and over moderate temperature excursions. Disadvantages of these resistors include relatively large size and poor dynamic characteristics because of their distributed nature. It is important to realize that the excellent temperature stability of these resistors can easily be negated if they are combined with components such as potentiometers for trimming. The accepted procedure when adjustments are required is to use shunt or series connections of selectable, stable resistors to closely approximate the required value. A potentiometer with a total range of a fraction of a percent of the desired value can then be used to complete the trim. The temperature coefficient of the relatively less stable element has little effect since the potentiometer resistance is a very small fraction of the total.

At least one manufacturer offers precision relatively thick metal-film resistors with tolerances to 0.005%. While the long-term stability and temperature coefficient of these units is not as good as that of the best wire wounds, their small size and excellent dynamic characteristics recommend them in many demanding applications.

The selection of acceptable capacitors is even more difficult. In addition to tolerance and stability problems, capacitors exhibit the phenomenon of *dielectric absorption*. One manifestation of this effect is that capacitors tend to "remember" and creep back toward the prior voltage if open circuited following a step voltage change. The time required to complete this transient ranges from milliseconds to thousands of seconds, while its magnitude can range from a fraction of a percent to as much as 25% of the original change, depending primarily on the capacitor dielectric material. Dielectric absorption deteriorates the performance of any circuit using capacitors, with sample and holds (where step voltage changes are routine) and integrators being particularly vulnerable.

Teflon and polystyrene are the best dielectric materials from the point of view of dielectric absorption. The dielectric-absorption coefficient (roughly equal to the fractional recovery following a step voltage change) can be less than 0.1% for capacitors properly constructed from these materials. They also have very high resistivity so that self-time constants (the product of capacitance and the shunt resistance that results from dielectric or case resistivity) in excess of 10^6 seconds are possible. While the temperature coefficient for either of these materials is normally the order of 100 parts per million per degree Centigrade, special processing or combinations of capacitors with two types of dielectrics can lower temperature coefficient to a few parts per million per degree Centigrade. The primary disadvantages are relatively large size and high cost (particularly for teflon) and a maximum temperature of 85° C for polystyrene.

Mica or glass capacitors often provide acceptable characteristics for lower-value units. Polycarbonate has considerably better volumetric efficiency than either teflon or polystyrene, and is used for moderate- and large-value capacitors. Dielectric absorption is somewhat poorer, but still acceptable in many applications. Mylar-dielectric capacitors are inexpensive and have an absorption coefficient of approximately 1%. These units are often used in noncritical applications.

Ceramic capacitors, particularly those constructed using high-dielectric-constant materials, have a particularly unfortunate combination of characteristics for most operational-amplifier circuits, and should generally be avoided except as decoupling components or in other locations where dielectric absorption is unimportant.

11.4 REPRESENTATIVE LINEAR CONNECTIONS

The objective of many operational-amplifier connections is to provide a linear gain or transfer function between circuit input and output signals. This section augments the collection of linear applications we have seen in preceding sections. As mentioned earlier, our objective in discussing these circuits is not to form a circuits handbook, but rather to encourage the creativity so essential to useful imaginative designs.

The connections presented in this and subsequent sections do not include the minor details that are normally strongly dependent on the specifics of a particular application and the operational amplifier used, and that would obscure more important and universal features. For example, no attempt is made to balance the resistances facing both input terminals, although we have seen that such balancing reduces errors related to amplifier input currents. We tacitly assume that the amplifier with feedback provides its ideal closed-loop gain unless specifically mentioned otherwise. Similarly, stability is assumed. The methods used to guarantee the latter assumption are the topic of Chapter 13.

11.4.1 Differential Amplifiers

We have seen numerous examples of both inverting and noninverting amplifier connections. Figure 11.10 shows a topology that combines the features of both of these connections. The ideal input-output relationship is easily determined by superposition. If V_b is zero,

$$V_o = -\frac{Z_2}{Z_1} V_a \tag{11.13}$$

If V_a is zero, the circuit is a noninverting amplifier preceded by an attenuator, and

$$V_o = \left(\frac{Z_4}{Z_3 + Z_4}\right)\left(\frac{Z_1 + Z_2}{Z_1}\right) V_b \tag{11.14}$$

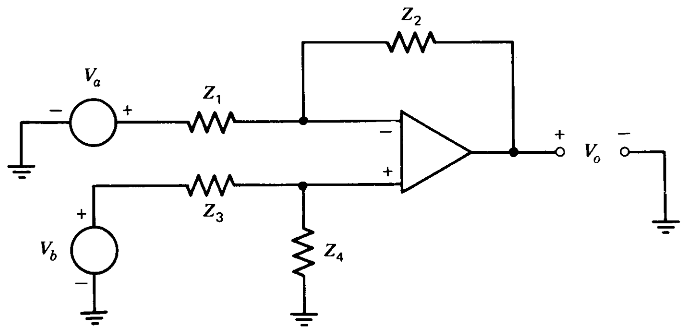


Figure 11.10 Differential connection.

Linearity insures that in general

$$V_o = \left(\frac{Z_4}{Z_3 + Z_4}\right)\left(\frac{Z_1 + Z_2}{Z_1}\right) V_b - \frac{Z_2}{Z_1} V_a \tag{11.15}$$

If values are selected so that $Z_4/Z_3 = Z_2/Z_1$.

$$V_o = \frac{Z_2}{Z_1}(V_b - V_a) \tag{11.16}$$

This connection is frequently used with four resistors to form a differential amplifier. Adjustment of any of the four resistors can be used to zero common-mode gain. Other possibilities involve combining two capacitors for Z_2 and Z_4 with two resistors for Z_1 and Z_3. If the time constants of the two combinations are equal, a differential or a noninverting integrator results.

It is important to note that the input current at the V_a terminal of the differential connection is dependent on both input voltages, while the current at the V_b terminal is dependent only on voltage V_b. This nonsymmetrical loading can cause errors in some applications. Two noninverting unity-gain amplifiers can be used as buffers to raise input impedance to very high levels if required.

If the design objective is a high-input-impedance differential amplifier with high common-mode rejection ratio, the connection shown in Fig. 11.11 can be used. Consider a common-mode input signal with $V_a = V_b = V_i$. In this case the two left-hand amplifiers combine to keep the voltage across R_2 zero. Thus for a common-mode input, the intermediate voltages V_c and V_d are related to inputs as

$$V_c = V_d = V_a \qquad V_a = V_b \tag{11.17}$$

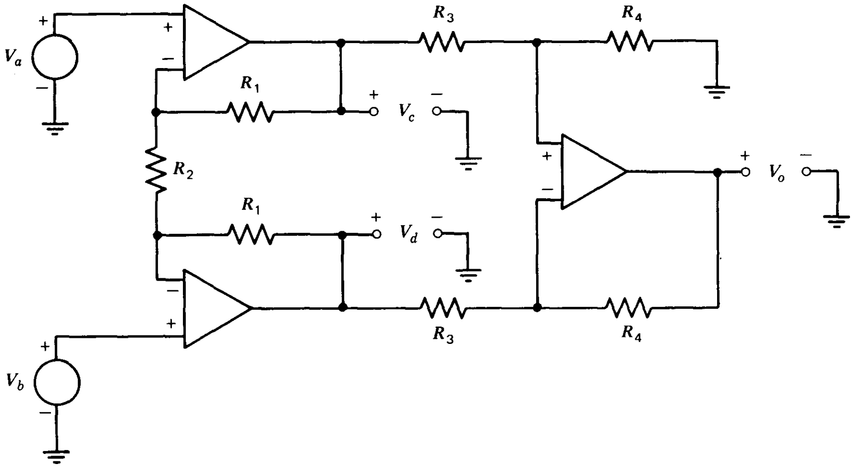


Figure 11.11 Buffered differential amplifier with high common-mode rejection ratio.

Alternatively, consider a pure differential input signal with $V_i/2 = V_a = -V_b$. In this case the midpoint of resistor R_2 is an incrementally grounded point, and each of the left-hand amplifiers functions as a noninverting amplifier with a gain of $(2R_1 + R_2)/R_2$. Linearity insures that the differential gain of the left-hand pair of amplifiers must be independent of common-mode level. Thus

$$\frac{V_c - V_d}{V_a - V_b} = \frac{2R_1 + R_2}{R_2} \tag{11.18}$$

The right-hand amplifier has a gain of zero for the common-mode component of V_c and V_d, and a gain of R_4/R_3 for the differential component of these intermediate signals. Combining expressions shows that V_o is independent of the common-mode component of V_a and V_b, and is related to these signals as

$$V_o = \left(\frac{2R_1 + R_2}{R_2}\right)\frac{R_4}{R_3}(V_a - V_b) \tag{11.19}$$

In addition to the high input impedance provided by the left-hand amplifiers, the differential gain of this pair makes the common-mode rejection of the overall amplifier less sensitive to ratio mismatches of the output-amplifier resistor networks.

11.4.2 A Double Integrator

We have seen that either inverting or noninverting integration can be accomplished with an operational amplifier. Figure 11.12 shows a connection that provides a second-order integration with a single operational amplifier. The circuit is analyzed by the virtual-ground method. Assuming that the inverting input of the amplifier is at ground potential

$$I_i(s) = \frac{V_i(s)}{2R(RCs + 1)} \tag{11.20}$$

and

$$I_f(s) = \frac{RC^2s^2V_o(s)}{2(RCs + 1)} \tag{11.21}$$

The negligible input current of the amplifier forces $I_f = -I_i$. Combining Eqns. 11.20 and 11.21 via this constraint shows that

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{(RCs)^2} \tag{11.22}$$

11.4.3 Current Sources

The operational amplifier can be used as a current source in a number of different ways. Figure 11.13 shows two simple configurations. In part *a* of this figure, the load serves as the feedback impedance of an inverting-connected operational amplifier. The virtual-ground method shows that the current through the load must be equal to the current through resistor *R*. In part *b*, the operational amplifier forces the voltage across *R* to be equal to the input voltage. Since the current required at the inverting input terminal of the amplifier is negligible, the load current is equal to the current through resistor *R*.

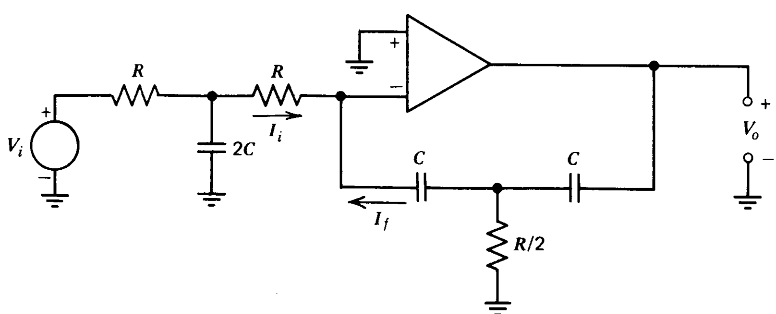


Figure 11.12 Double integrator.

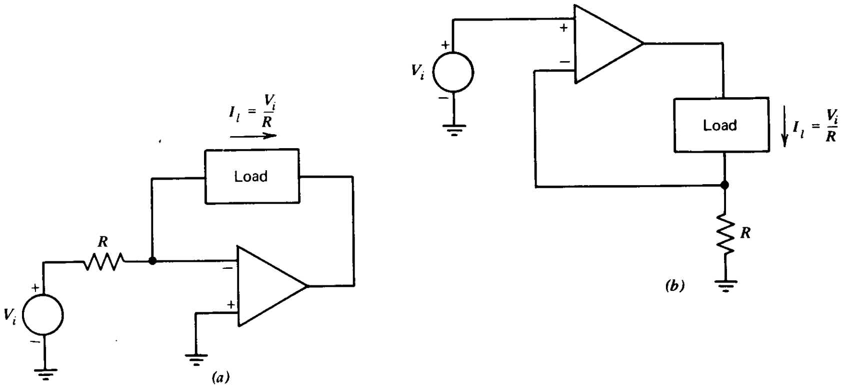


Figure 11.13 Current sources. (*a*) Inverting connection. (*b*) Follower connection.

Both of the current-source connections described above require that the load be floating. The configuration shown in Fig. 11.14 relaxes this requirement. Here the operational amplifier constrains the source current of a field-effect transistor. Provided that operating levels are such that the FET gate is reverse biased, the source and drain currents of this device are identical. Thus the operational amplifier controls the load current indirectly.

The relative operating levels of the circuit shown in Fig. 11.14 must be constrained to keep the FET in its forward operating region with its gate

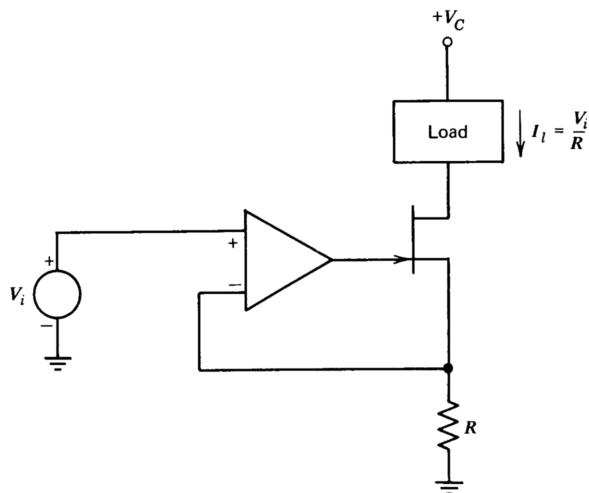


Figure 11.14 Current source using a field-effect transistor.

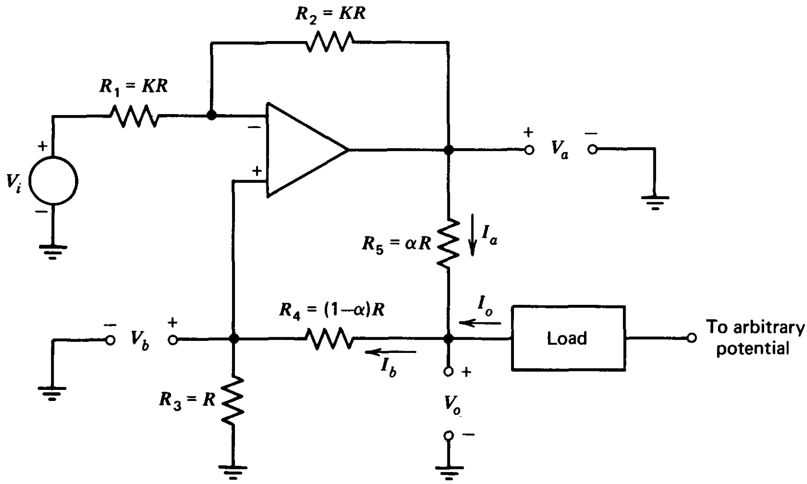


Figure 11.15 Howland current source.

reverse biased for satisfactory performance. The Howland current source shown in Fig. 11.15 allows further freedom in the choice of operating levels.

The analysis of this circuit is simplified by noting that the operational amplifier relates V_a to V_i and V_b as

$$V_a = -V_i + 2V_b \tag{11.23}$$

The circuit topology implies the relationships

$$I_o = I_b - I_a \tag{11.24}$$

$$I_a = \frac{V_a - V_o}{\alpha R} \tag{11.25}$$

$$I_b = \frac{V_o - V_b}{(1 - \alpha)R} \tag{11.26}$$

and

$$V_b = \frac{V_o}{2 - \alpha} \tag{11.27}$$

The transfer relationships of interest for this circuit are the input voltage to short-circuit output current transconductance I_o/V_i and the output conductance of the circuit I_o/V_o. Solving Eqns. 11.23 through 11.27 for these conductances shows that

$$\left.\frac{I_o}{V_i}\right|_{V_o = 0} = \frac{1}{\alpha R} \tag{11.28}$$

and

$$\left.\frac{I_o}{V_o}\right|_{V_i = 0} = 0 \tag{11.29}$$

Since the output current is independent of output voltage, we can model the circuit as a current source with a magnitude dependent on input voltage.

While the output resistance of this current source is independent of the quantity α, this parameter does affect scale factor. Smaller values of αR also allow a greater maximum output current for a given output voltage saturation level from the operational amplifier. There is a tradeoff involved in the selection of α, however, since smaller values for this parameter result in higher error currents for a given offset voltage referred to the input of the amplifier (see Problem P11.11).

There is further freedom in the selection of relative resistor ratios, since an extension of the above analysis shows that the output resistance is infinite provided $R_2/R_1 = (R_4 + R_5)/R_3$.

It is interesting to note that the success of this current source actually depends on *positive* feedback. Consider a voltage V_o applied to the output terminal of the circuit. The current that flows through resistor R_4 is exactly balanced by current supplied from the output of the operational amplifier via resistor R_5. The voltage at the output of the operational amplifier is the same polarity as V_o and has a larger magnitude than this variable.

We should further note that the resistor R_3 does not have to be connected to ground, but can also function as an input terminal. In this configuration the output current is proportional to the difference between the voltages applied to the two inputs.

11.4.4 Circuits which Provide a Controlled Driving-Point Impedance

We have seen examples of circuits designed to produce very high or very low input or output impedances. It is also possible to use operational amplifiers to produce precisely controlled output or driving-point impedances. Consider the circuit shown in Fig. 11.16. The operational amplifier is configured to provide a noninverting gain of two. As a result of this gain, the impedance connected between the amplifier output and its noninverting input has a voltage V_i across it with a polarity as shown in Fig. 11.16. Since there is negligible current required at the inverting input of the amplifier, the input current required from the source is

$$I_i = -I_a = -\frac{V_i}{Z} \tag{11.30}$$

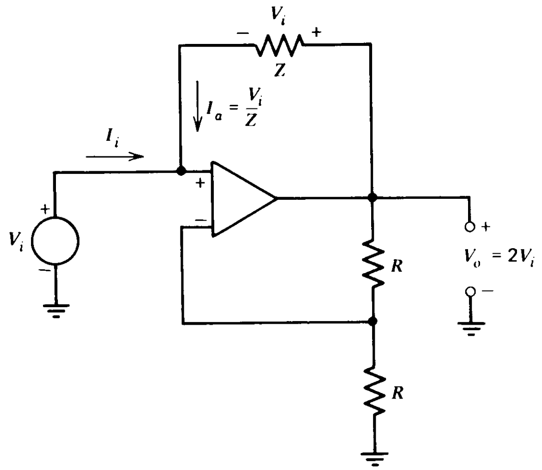


Figure 11.16 Negative impedance converter.

Solving Eqn. 11.30 for the input impedance of the circuit yields

$$\frac{V_i}{I_i} = -Z \tag{11.31}$$

Equation 11.31 shows that this circuit has sufficient positive feedback to produce negative input impedances.

The gyrator shown in Fig. 11.17 is another example of a circuit that provides a controlled driving-point impedance. The circuit relationships include

$$I_i = I_a + I_b \tag{11.32}$$

$$I_a = \frac{V_i - V_a}{R_1} = \frac{-V_i}{R_1} \tag{11.33}$$

$$I_b = \frac{V_i - V_b}{R_1} \tag{11.34}$$

$$V_b = -\frac{V_i Z}{R_2} \tag{11.35}$$

Combining Eqns. 11.32 through 11.35 and solving for the driving-point impedance shows that

$$\frac{V_i}{I_i} = \frac{R_1 R_2}{Z} \tag{11.36}$$

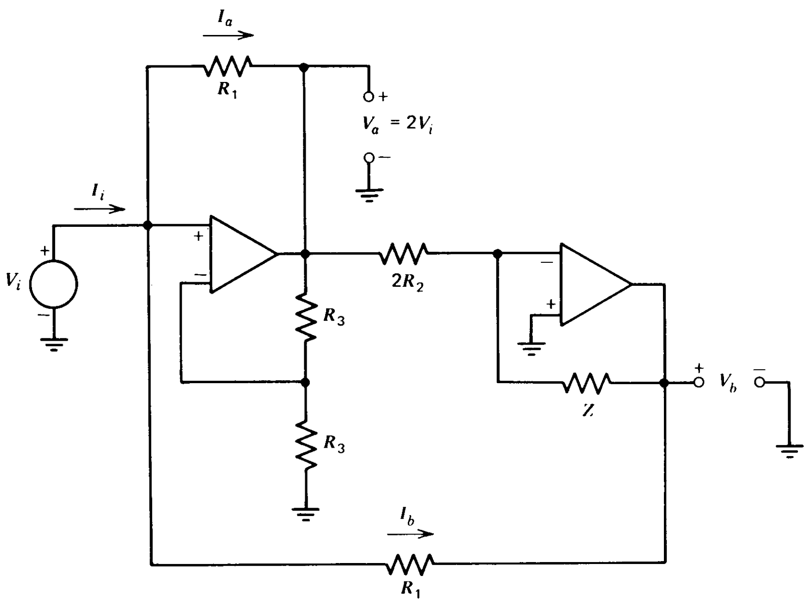


Figure 11.17 Gyrator.

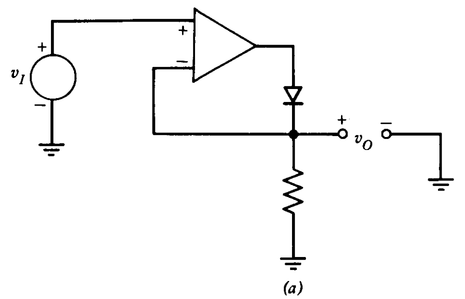
We see that the gyrator provides a driving-point impedance that is reciprocally related to another circuit impedance. Applications include the synthesis of elements that function as inductors using only capacitors, resistors, and operational amplifiers. For example, if we choose impedance Z to be a 1-μF capacitor and $R_1 = R_2 = 1$ kΩ, the driving-point impedance of the circuit shown in Fig. 11.17 is s, equivalent to that of a 1-henry inductor.

11.5 NONLINEAR CONNECTIONS

The topologies presented in Section 11.4 were intended to provide linear gains, transfer functions, or impedances. While practical realizations of these circuits may include nonlinear elements, the feedback is arranged to minimize the effects of such nonlinearities. In many other cases feedback implemented by means of operational amplifiers is used to augment, control, or idealize the characteristics of nonlinear elements. Examples of these types of applications are presented in this section.

11.5.1 Precision Rectifiers

Many circuit connections use diodes to rectify signals. However, the forward voltage drop associated with a diode limits its ability to rectify low-



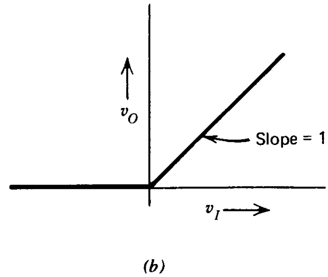


Figure 11.18 Precision rectifier. (*a*) Circuit. (*b*) Transfer characteristics.

level signals. The combination of a diode with an operational amplifier (Fig. 11.18) results in a circuit with a much lower threshold. Operation depends on the fact that the diode-amplifier combination can only pull the output voltage positive, so that negative input voltages result in zero output. With a positive input voltage, a negligibly small differential signal (equal to the threshold voltage of the diode divided by the open-loop gain of the amplifier) is amplified to provide sufficient amplifier output voltage to overcome the diode threshold, with the result that

$$v_O = v_I \qquad v_I > 0 \tag{11.37a}$$

$$v_O = 0 \qquad v_I < 0 \tag{11.37b}$$

Many variations of this precision rectifier or "superdiode" exist. For example, the circuit shown in Fig. 11.19 rectifies and provides a current-source drive for a floating load such as a D'Arsonval meter movement. Figure 11.20 illustrates another rectifier circuit. With v_I negative, voltage v_A is zero, and $v_O = -v_I$ because of the inversion provided by the right-hand amplifier. The transistor provides a feedback path for the first amplifier so that it remains in its linear region for negative inputs. Operation in the linear region keeps the inverting input of the first amplifier at ground potential, thereby preventing the input signal from driving voltage v_A via direct resistive feedthrough. Maintaining linear-region operation also eliminates the long amplifier recovery times that frequently accompany overload and saturation. While a diode could be used in place of the transistor, the transistor provides a convenient method for driving further amplifying circuits, which indicate input-signal polarity if this function is required. For positive input voltages, voltage $v_A = -v_I$, so that the resistor with value

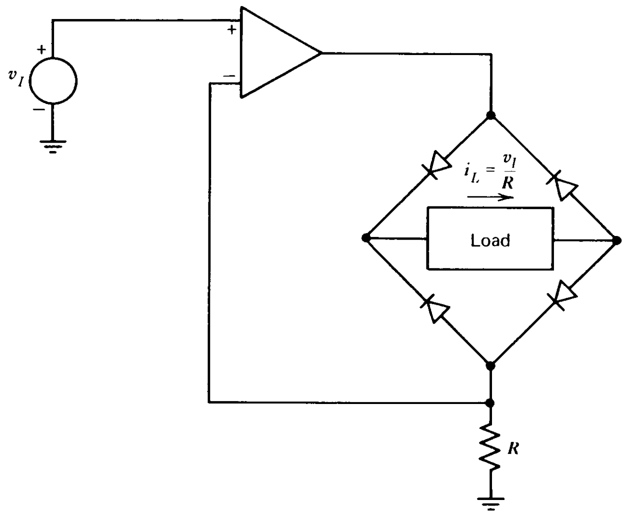


Figure 11.19 Full-wave precision rectifier for floating load.

$R/2$ also applies current to the input of the second amplifier, with the result that

$$v_O = -(v_I - 2v_I) = v_I \qquad v_I > 0 \tag{11.38a}$$

$$v_O = -v_I \qquad v_I < 0 \tag{11.38b}$$

11.5.2 A Peak Detector

The peak-detector circuit shown in Fig. 11.21 illustrates a further elaboration on the general theme of minimizing the effects of voltage drops in various elements by including these drops inside a feedback loop. If the output voltage is more positive than the input voltage, the output of the operational amplifier will be saturated in the negative direction. (Some form of clamping may be included to speed recovery from this state.) Under these conditions, the capacitor current consists only of diode and FET-gate leakage currents; thus the capacitor voltage changes very slowly. As a matter of practical concern, the circuit will function properly only if current levels are such that the capacitor voltage drifts negatively in this state. Otherwise, the connection will eventually saturate at its maximum positive output level.

If v_I becomes greater than v_O, the capacitor is charged rapidly from the output of the operational amplifier via the diode until equality is reestablished. Note that the capacitor voltage is not forced to be equal to v_I, but

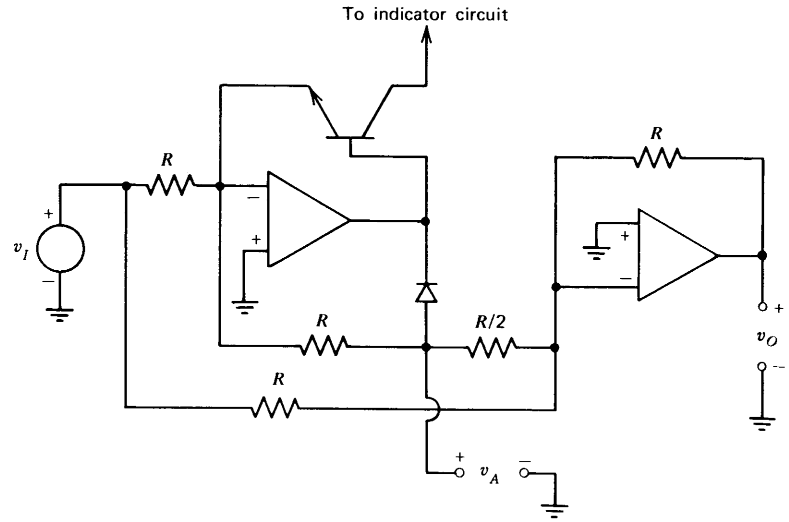


Figure 11.20 Full-wave precision rectifier.

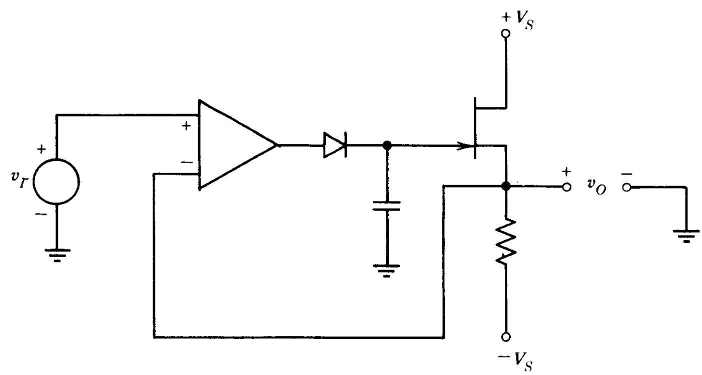


Figure 11.21 Peak detector.

rather to be equal to a voltage that, combined with the FET gate-to-source voltage, forces equality between v_O and v_I. In this way the output voltage "remembers" the most positive value of the input signal.

11.5.3 Generation of Piecewise-Linear Transfer Characteristics

Diodes can be combined with operational amplifiers to realize signal-shaping circuits other than rectifiers. Figure 11.22 shows a circuit that provides a compressive or limiting-type nonlinear transfer relationship. For

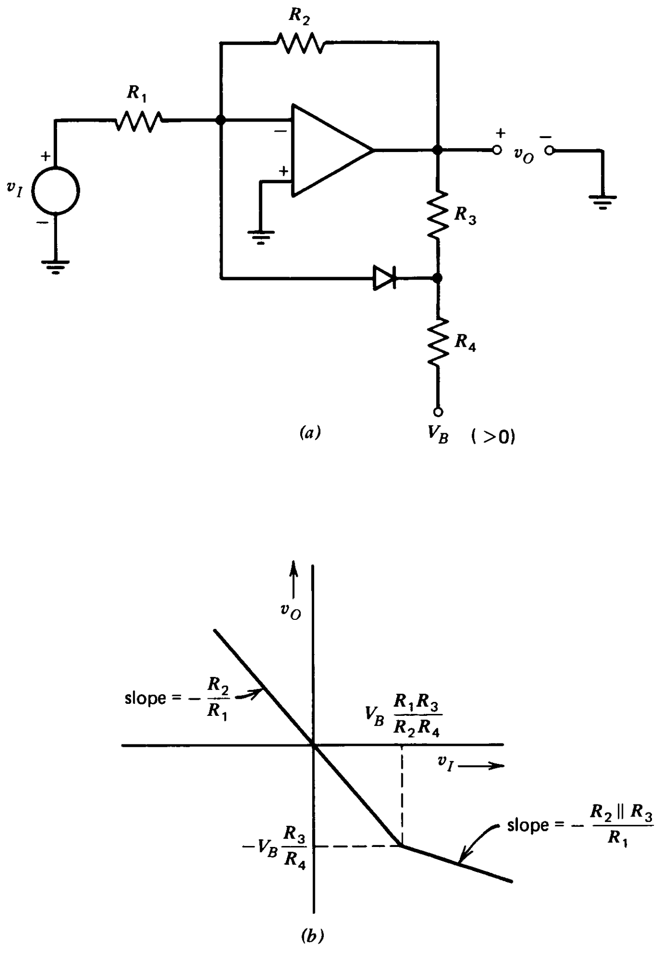


Figure 11.22 Limiter. (*a*) Circuit. (*b*) Transfer characteristics.

input voltages more negative than $V_B(R_1R_3/R_2R_4)$ the diode is an open circuit, and the incremental gain of the circuit is $-R_2/R_1$. When $v_I = V_B(R_1R_3/R_2R_4)$, the diode is on the threshold of conduction. Assuming a "perfect" diode (zero threshold voltage and zero on resistance in the forward direction), the effective feedback resistance for further increases in input voltage is $R_2 \parallel R_3$, and the magnitude of the incremental gain decreases to $-(R_2 \parallel R_3)/R_1$.

The operation of the limiter was described assuming perfect diode characteristics. If the performance degradation that results from actual diode characteristics is intolerable, a "superdiode" connection can be used as shown in Fig. 11.23. The lower operational amplifier cannot affect circuit operation for the positive values of v_A that correspond to input voltages more negative than $V_B(R_1R_3/R_2R_4)$ because the diode in series with its output is reverse biased. However, the lower amplifier can supply as much current as is required to keep the voltage at the junction of R_3 and R_4 from becoming negative, and thus this circuit provides hard limiting with the incremental gain dropping to zero for input voltages more positive than the threshold level. If softer limiting is required, a resistor can be included at the indicated point.

It is clear that additional resistor networks and diodes (or superdiodes) can be added to increase the number of break points in the transfer characteristics. However, the topology of Fig. 11.22 or Fig. 11.23 precludes increasing the magnitude of the incremental gain as input-voltage magnitude increases. Shifting the diode-resistor network to the amplifier input circuit (Fig. 11.24) is one way that expansive-type nonlinearities can be realized.

11.5.4 Log and Antilog Circuits

The exponential current-voltage characteristics of diodes or transistors can be exploited to realize circuits with exponential or logarithmic characteristics. Figure 11.25 illustrates a very simple circuit that provides a logarithmic relationship between output voltage and input current. Under normal operating conditions, the operational amplifier keeps the collector-to-base voltage of the transistor at zero. As a result, collector-to-base junction leakage currents are eliminated as are base-width modulation effects, and many types of transistors will accurately follow the relationship

$$i_C \simeq I_S e^{qv_{BE}/kT} \tag{11.39}$$

over a range of operating current levels that extends from picoamperes to a fraction of a milliamp. Deviation from purely exponential behavior oc-

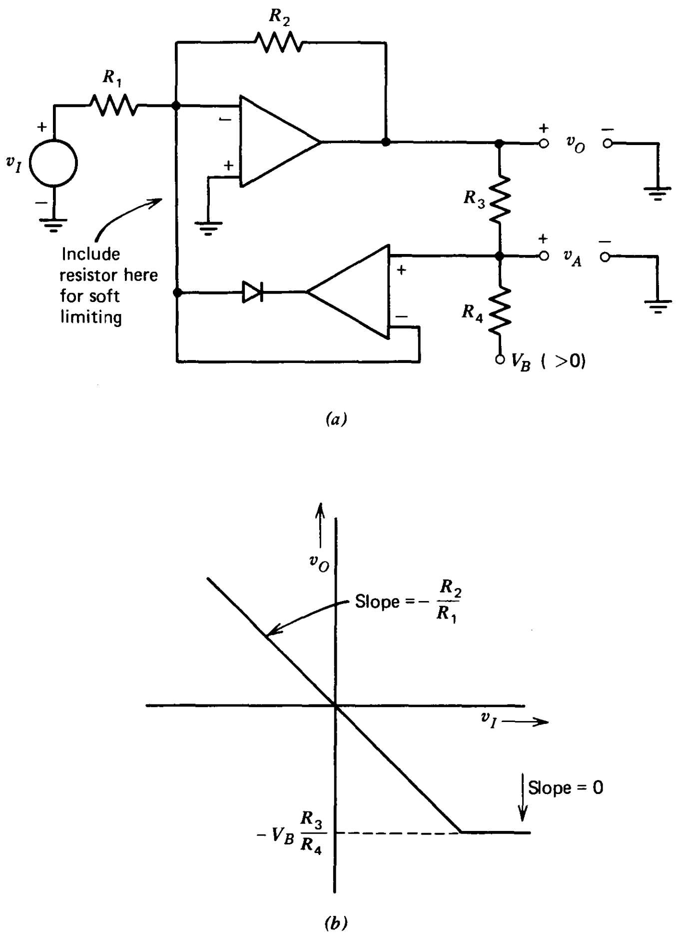
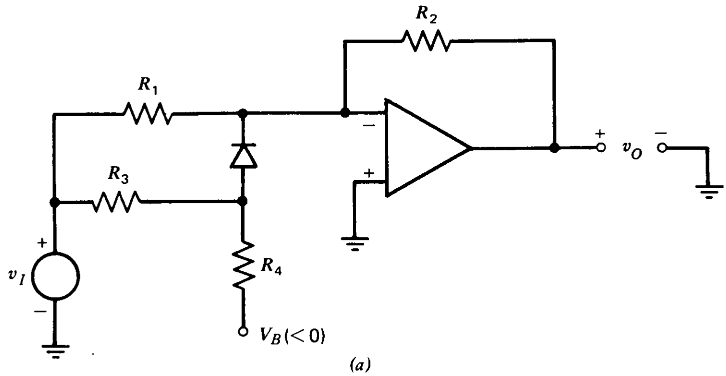


Figure 11.23 Limiter incorporating a super diode. (*a*) Circuit. (*b*) Transfer characteristics.



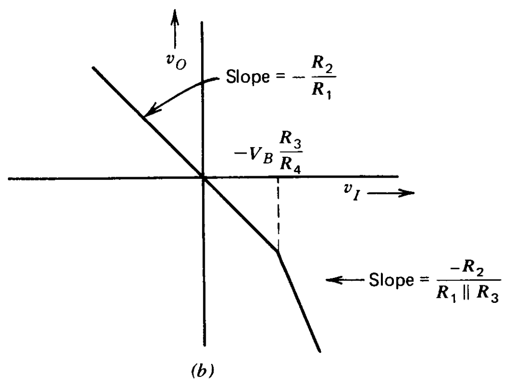


Figure 11.24 Expander. (*a*) Circuit. (*b*) Transfer characteristics.

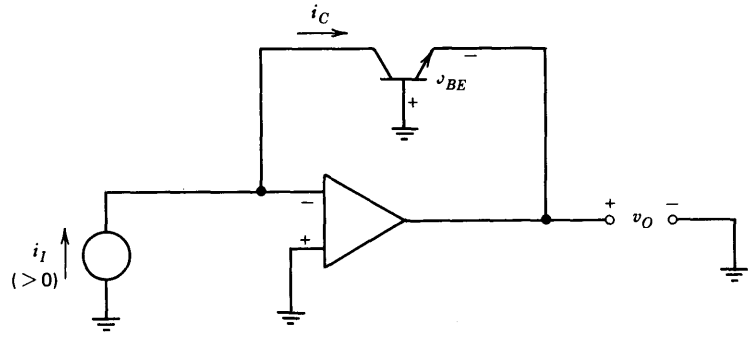


Figure 11.25 Log circuit.

curs at current levels comparable to I_S and at current levels where ohmic resistances become significant.[4]

For this circuit topology, $v_{BE} = -v_O$, and feedback keeps $i_C = i_I$. Substituting these constraints into Eqn. 11.39 shows that

$$i_I = I_S e^{-qv_O/kT} \tag{11.40}$$

or, if we solve for v_O,

$$v_O = -\frac{kT}{q} \ln \frac{i_I}{I_S} \tag{11.41}$$

Of course, the current applied to this circuit can be derived from an available input voltage via a resistor connected to the inverting input terminal of the operational amplifier. In this case, the voltage offset of the operational amplifier contributes an error term that normally limits dynamic range to three or four orders of magnitude. If the input signal is available as a current, as it is for some sensors such as ionization gauges, much wider dynamic range is possible for sufficiently low amplifier bias current.

One shortcoming of this simple circuit is that the quantity I_S is highly temperature dependent (see Section 7.2). The circuit shown in Fig. 11.26 offers improved performance with temperature. Feedback through the right-hand operational amplifier keeps the collector current of Q_2 equal to the reference current I_R; thus

$$v_{BE2} = \frac{kT}{q} \ln \frac{I_R}{I_{S2}} \tag{11.42}$$

[4] Theoretically, a diode could be used as a feedback element as indicated in Section 1.2.3 to obtain logarithmic closed-loop characteristics. In practice, the transistor connection illustrated here is preferable, since transistors generally display the desired characteristics over a far larger dynamic range than do diodes.

Note that, since the potential at the collector of Q_2 is held at zero volts by the operational amplifier, the reference current is easily obtained via a resistor connected to a positive supply voltage.

The left-hand operational amplifier adjusts the base voltage of Q_2, thereby changing the base-to-emitter voltage of Q_1 until the collector current of Q_1 equals i_I, with the result that

$$v_{BE1} = \frac{kT}{q} \ln \frac{i_I}{I_{S1}} \tag{11.43}$$

If values are selected so that the base current of Q_2 does not load the base-circuit attenuator, the voltage relationship is

$$v_{BE1} = v_{BE2} - \frac{1}{16.7} v_O \tag{11.44}$$

Combining Eqns. 11.42 through 11.44 and solving for v_O yields

$$v_O = -16.7 \frac{kT}{q} \left[\ln \frac{i_I}{I_{S1}} - \ln \frac{I_R}{I_{S2}} \right] = -16.7 \frac{kT}{q} \ln \left[\frac{i_I}{i_R} \frac{I_{S2}}{I_{S1}} \right] \tag{11.45}$$

If transistors Q_1 and Q_2 have well-matched values of I_S, Eqn. 11.45 becomes

$$v_O = -16.7 \frac{kT}{q} \ln \left[\frac{i_I}{i_R} \right] \tag{11.46}$$

The resistive-divider attenuation ratio of 16.7 is used so that at room temperature, Eqn. 11.46 reduces to

$$v_O = -1 \text{ volt} \log_{10} \left[\frac{i_I}{i_R} \right] \tag{11.47}$$

While the use of matched transistors as shown in Fig. 11.26 does eliminate the dependence of the output on I_S, Eqn. 11.46 shows that the scale factor of the circuit is proportional to absolute temperature. One common solution is to compensate by using a resistor with a value inversely proportional to absolute temperature as the smaller of the two resistors in the voltage divider.

The antilog circuit shown in Fig. 11.27 results from rearranging components. The reader should verify that, at room temperature and with matched transistors, the input-output relationship for this circuit is

$$v_O = R_1 I_R \times 10^{-(v_I/1 \text{ volt})} \tag{11.48}$$

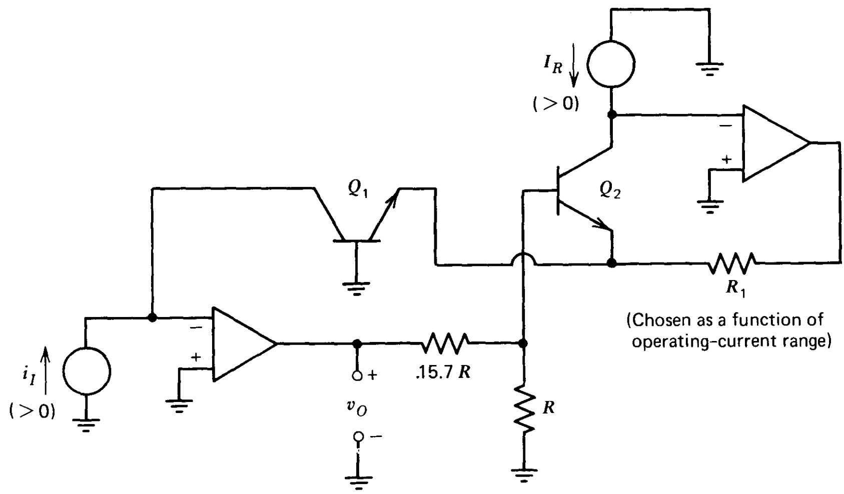


Figure 11.26 Improved log circuit.

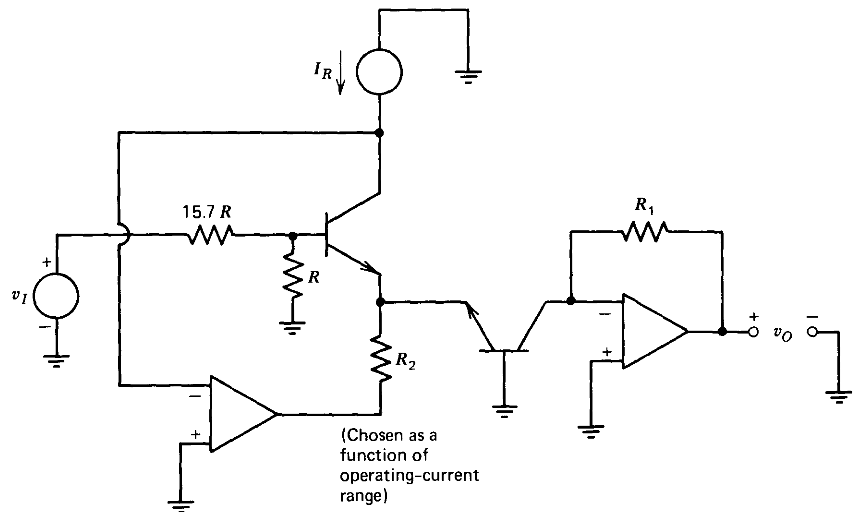


Figure 11.27 Antilog circuit.

11.5.5 Analog Multiplication

There are a number of configurations that perform analog multiplication, that is, provide an output voltage proportional to the product of two input voltages. For example, one or more log circuits can be combined with an antilog circuit to realize multipliers, dividers, or circuits that raise a voltage to a power. Another technique known as quarter-square multiplication exploits the relationship

$$(v_X + v_Y)^2 - (v_X - v_Y)^2 = 4v_Xv_Y \tag{11.49}$$

The quadratic transfer characteristics can be approximated with piecewise-linear diode-operational amplifier connections.

A method known as transconductance multiplication is the basis for several available discrete and integrated-circuit analog multipliers because it is capable of moderate accuracy and requires relatively few components. A simplified transconductance multiplier (limited to two-quadrant operation because the voltage v_Y cannot be negative) is shown in Fig. 11.28.

If it is assumed the v_X attenuator is not loaded by the input current of transistor Q_1 and that the differential input voltage applied to the pair is small enough so that linear-region relationships are valid for the transistors, the difference between the two collector currents is

$$i_{C1} - i_{C2} = \alpha v_X g_m \tag{11.50}$$

where g_m is the (equal) transconductance of either transistor.

For small-signal operation, the quantity g_m is related to quiescent operating current, which is in turn determined by the input variable v_Y. Thus,

$$g_m = \frac{i_Y q}{2kT} = \frac{Kv_Y q}{2kT} \tag{11.51}$$

Substituting Eqn. 11.51 into Eqn. 11.50 shows that

$$i_{C1} - i_{C2} = \frac{\alpha Kq}{2kT} v_Xv_Y \tag{11.52}$$

The reader should convince himself that the differentially connected operational amplifier provides an output voltage equal to R_2 times the difference between the two collector currents. Substituting this relationship into Eqn. 11.52 yields

$$v_O = \frac{\alpha KR_2q}{2kT} v_Xv_Y \tag{11.53}$$

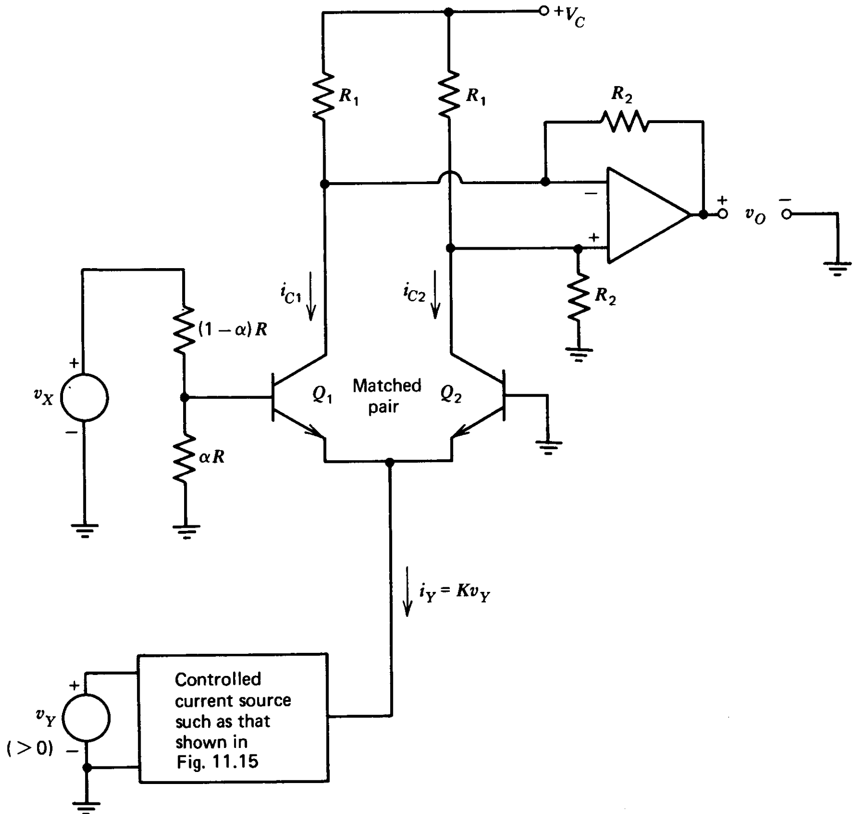


Figure 11.28 Two-quadrant transconductance multiplier.

There are a number of design constraints necessary for satisfactory operation or introduced for convenience, including the following.

(a) The current i_Y is normally limited to a fraction of a milliamp so that performance is not degraded by ohmic transistor resistance.

(b) The attenuation ratio α must be chosen to limit the input voltage applied to the transistor pair to a low level. Detailed calculations show that the inaccuracy attributable to the exponential transistor characteristics can be limited to less than 1% of maximum output if the maximum magnitude of the voltage into the differential pair is kept below approximately 8 mV.

(c) Because of the limited signal levels applied to the differential pair, its drift has a significant effect on overall performance. The circuit can be balanced by adjusting the ratio of the two resistors labeled R_1 in Fig. 11.28.

(d) The temperature dependence of Eqn. 11.53 can be compensated for by making the voltage-attenuator ratio or the current-source scale factor temperature dependent.

(e) The restriction of single-polarity values for the v_Y input can be removed by including a second differential pair of transistors, and by making the operating currents of the two pairs vary differentially as a function of v_Y. The interested reader is invited to show that the input-output relationship for the four-quadrant transconductance multiplier shown in Fig. 11.29 is given by Eqn. 11.53.

(f) Scale factor is frequently adjusted to give $v_O = v_X v_Y/10$ volts, a value compatible with the signal levels common to many analog systems.

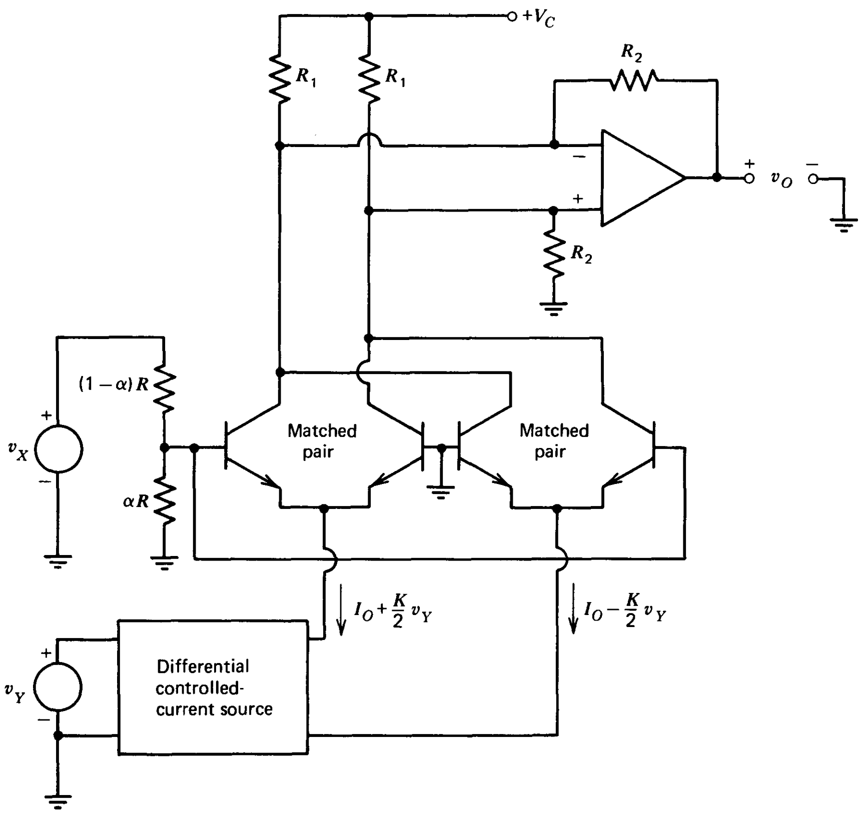


Figure 11.29 Four-quadrant transconductance multiplier.

In general, achieving highly accurate performance from a transconductance multiplier involves a rather complex series of adjustments to null various sources of error. This process is simplified somewhat by an innovation developed by Gilbert[5] which uses compensating diodes to eliminate scale-factor temperature dependence and to increase the signal levels that may be applied to the differential pairs. While there are problems that must be overcome, the technique is good enough so that several manufacturers offer inexpensive transconductance multipliers with errors from all sources of less than 1% of maximum output.

11.6 APPLICATIONS INVOLVING ANALOG-SIGNAL SWITCHING

Systems that combine operational amplifiers with analog switches add a powerful dimension to the data-processing capability of the amplifiers alone. The switches are often used to control analog operations with digital command signals, and the resultant *hybrid* (analog-digital) circuits such as analog-to-digital converters are used in a myriad of applications. While a detailed discussion of these advanced techniques is beyond the scope of this book, several simple examples of connections including analog switching are presented in this section.

Either junction-gate or MOS field-effect transistors are frequently used for low-level signal switching. One advantage of a field-effect transistor as an analog switch is that it has no inherent offset voltage. The drain-to-source characteristics of a FET in the on state are linear and resistive for small channel currents, and the drain-to-source voltage is zero for zero channel current. A second advantage is that the channel leakage current of a pinched-off FET is generally under 1 nA at room temperature. This level is insignificant in many operational-amplifier connections.

There are several integrated circuits available that combine FET's with drive circuitry to interface the switch to digital-signal levels. Alternatively, discrete-component circuits can be designed to take advantage of the lower on-state resistances generally available from discrete field-effect transistors.

A second possibility is to use a bipolar transistor as a switch. The current handling capacity of bipolar devices is generally higher than that of FET's. However, there is a collector-to-base offset voltage that can be as

[5] B. Gilbert, "A D.C.-500 MHz Amplifier/Multiplier Principle," Digest of Technical Papers, 1968 Solid-State Circuits Conference, Philadelphia, Pa.

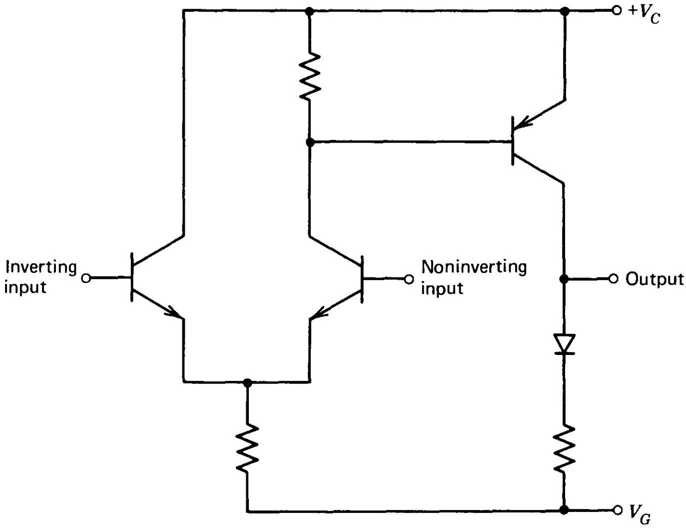


Figure 11.30 Gated operational amplifier.

high as several hundred millivolts.[6] Some high-current switching techniques arrange the feedback to eliminate offset-voltage effects.

A third type of switch combines the switching and amplification functions in a single circuit. Figure 11.30 shows a possible connection. With V_G negative, the amplifier is an example of the simple two-stage topology described in Section 8.2.3. If voltage V_G is switched to a positive potential, all three transistors and the diode become reverse biased, and thus both inputs and the output are open circuits. The gating feature can be retained in designs that expand the simple configuration shown in Fig. 11.30 into a complete operational amplifier. Several integrated-circuit examples of this type of design exist (see Section 10.4.2).

[6] One way to reduce the offset voltage of a bipolar transistor is to use it in an inverted or reverse mode with the roles of the emitter and collector interchanged, and offset voltages of a fraction of a millivolt are possible in this connection. The reason for the lower offset in the inverted mode is that the collector-to-emitter voltage of a saturated transistor is, in the absence of ohmic drops,

$$V_{\text{offset}} = \frac{kT}{q} \ln \frac{1}{\alpha}$$

The reverse common-base current gain α_R is used to determine forward-region offset, while the forward gain α_F is used to determine inverted offset voltage. Since α_F is generally close to one, inverted offset voltages can be quite small. Unfortunately, current gain and breakdown voltages are usually limited in the inverted connection. Consequently, as FET characteristics have improved, these devices have largely replaced inverted bipolar transistors as low-level switches.

One frequent use for analog switching is to multiplex a number of signals. The required circuit can be realized by using field-effect transistors to switch the signal applied to the input of a noninverting buffer amplifier. Another topology (see Fig. 11.31) results in an inverting multiplexer. The advantage of this configuration is that the drive circuit can be simpler than is the case with the noninverting connection. Recall that for a junction FET, it is necessary to make the gate potential approximately equal to the channel potential to turn on the transistor. If the noninverting connection is used, the channel of the on FET will be at the potential of the selected input. Furthermore, one end of the channel of all other switches will also be at the potential of the selected input. These uncertain levels complicate the drive-circuit requirements.

In the inverting topology, the channel of the on FET will be close to ground, and the diodes shown in Fig. 11.31 insure that the drain of the off FET will not be significantly more negative than ground. Thus a switch is turned on by grounding its gate, and turned off by making its gate more negative than the pinchoff voltage. An example of a common-base level shifter that converts T^2L logic signals to the required gate-drive levels is described in Section 12.3.3.

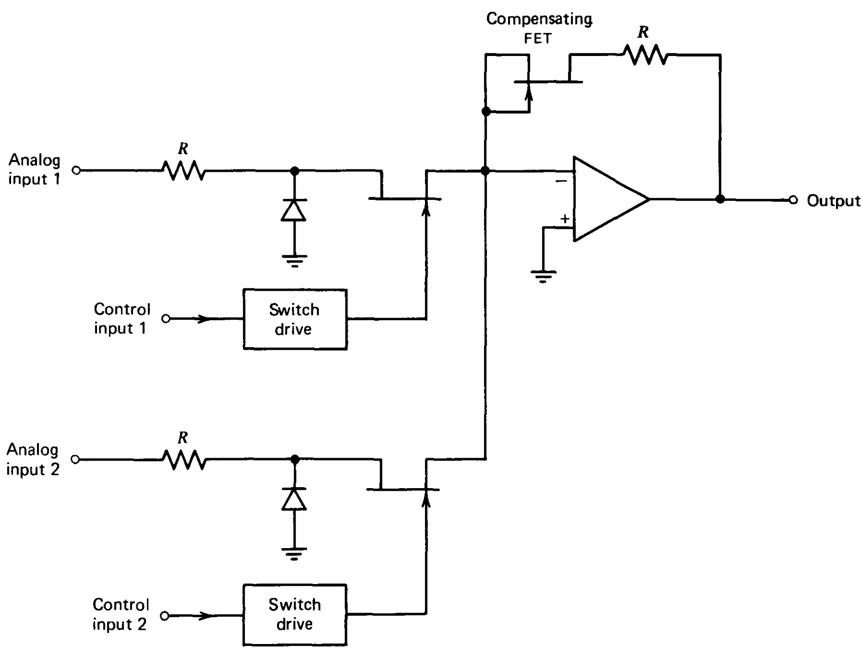


Figure 11.31 Inverting multiplexer.

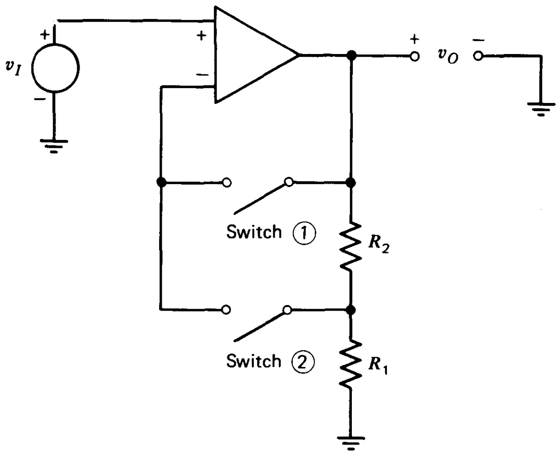


Figure 11.32 Gain-range amplifier.

The compensating FET is selected to have an on resistance matched to that of the switches. This device keeps the gain of the multiplexer equal to -1 as on resistance changes with temperature.

There are a variety of applications that require an amplifier with a selectable closed-loop gain. One topology for this type of gain-range amplifier is shown in Fig. 11.32. With switch ① closed and switch ② open, the ideal closed-loop gain is one, while reversing the state of the two switches changes the ideal gain to $(R_1 + R_2)/R_1$. The on resistance of the switches is relatively unimportant because only the low input current of the operational amplifier flows through a switch in this connection.

A related circuit function is that of an amplifier that provides a selectable gain of plus or minus one. One use for this kind of circuit is in square-wave modulators or demodulators. Figure 11.33 illustrates a possible connection. Assume initially the switch ② is not included in the circuit. With switch ① closed, the amplifier provides an ideal closed-loop gain of -1. With switch ① open, the voltage $v_A = v_I$, and thus the circuit provides an ideal gain of $+1$.

Switch ② may be included to reduce the effects of switch on-state resistance. Assume, for example, that design considerations dictate a value for R_1 equal to 10^3 times the on-state resistance of a switch. If only switch ① is used, a closed-loop gain error of 0.2% results from this resistance with the switch closed. If both switches are included and closed, the voltage v_A is reduced by a factor of 2.5×10^5 relative to v_I because of the resulting two stages of attenuation. This attenuation lowers the error from feedthrough to an insignificant level.

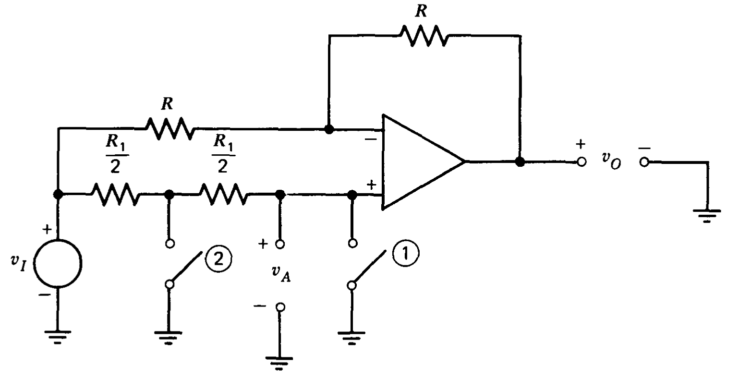


Figure 11.33 Amplifier that provides gain of ± 1.

There are a number of topologies that combine operational amplifiers with switches to form a sample-and-hold circuit. Figure 11.34 shows one possibility. When the FET conducts, the loop drives the voltage v_O toward the value of v_I. The complementary emitter-follower pair amplifies the limited current available from the operational amplifier and FET combination so that large currents can be supplied to the capacitor to charge it rapidly. The resistive path between bases and emitters of the follower pair

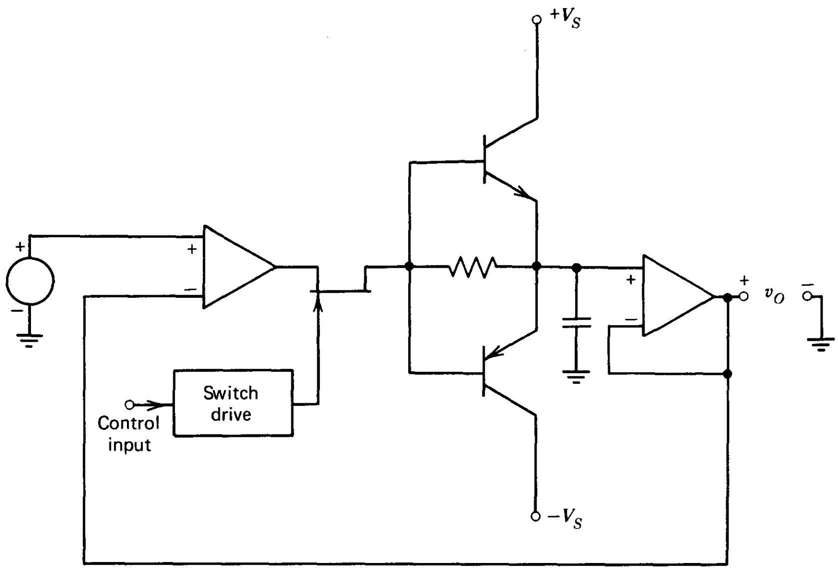


Figure 11.34 Sample-and-hold circuit.

eliminates the deadzone, which would result near equilibrium if the transistors alone were used. While the gain of the first operational amplifier insures that such a deadzone would not influence static characteristics, it could deteriorate stability.

When the switch opens, current into the capacitor is limited to buffer-amplifier input current and switch and emitter-follower leakage current. The base-to-emitter resistor prevents amplification of leakage currents in this state. Since the total capacitor current in the hold mode can be kept small, the held voltage maintains the desired value for prolonged periods.

Note that a field-effect transistor could be used as a buffer as was done in the peak detector described in Section 11.5.2 since the high open-loop gain of the first amplifier would drive the capacitor voltage to the value necessary to make $v_O = v_I$. However, the output resistance is higher in the hold mode if the FET buffer is used, since feedback is not available to reduce output impedance in the hold mode.

PROBLEMS

P11.1

The following results are obtained for measurements made using the circuit shown in Fig. 11.35*a*.

1. With switch ① open and switch ② closed, $V_O = 12$ mV.
2. With switch ① closed and switch ② closed, $V_O = 32$ mV.
3. With switch ① closed and switch ② open, $V_O = 10$ mV.

Determine values for the three bias generators shown in Fig. 11.35*b*. In this representation, the external generators model all bias voltage and current effects so that the input currents and differential input voltage at the terminals of the amplifier shown in the model are zero.

The amplifier is connected as shown in Fig. 11.35*c*. Express v_O in terms of v_I and the amplifier parameters shown in Fig. 11.35*b*.

P11.2

The circuit shown in Fig. 11.2*a* is used to measure the input offset voltage of an operational amplifier with a d-c open-loop voltage gain of 10^4. What error does limited loop transmission introduce into the offset measurement for these parameter values?

P11.3

A certain operational amplifier is specified to have a maximum input offset voltage magnitude of 5 mV. The amplifier is connected as a unity-gain inverter using two 2-MΩ resistors. The noninverting input is connected directly to ground. Measurements reveal that the output voltage is

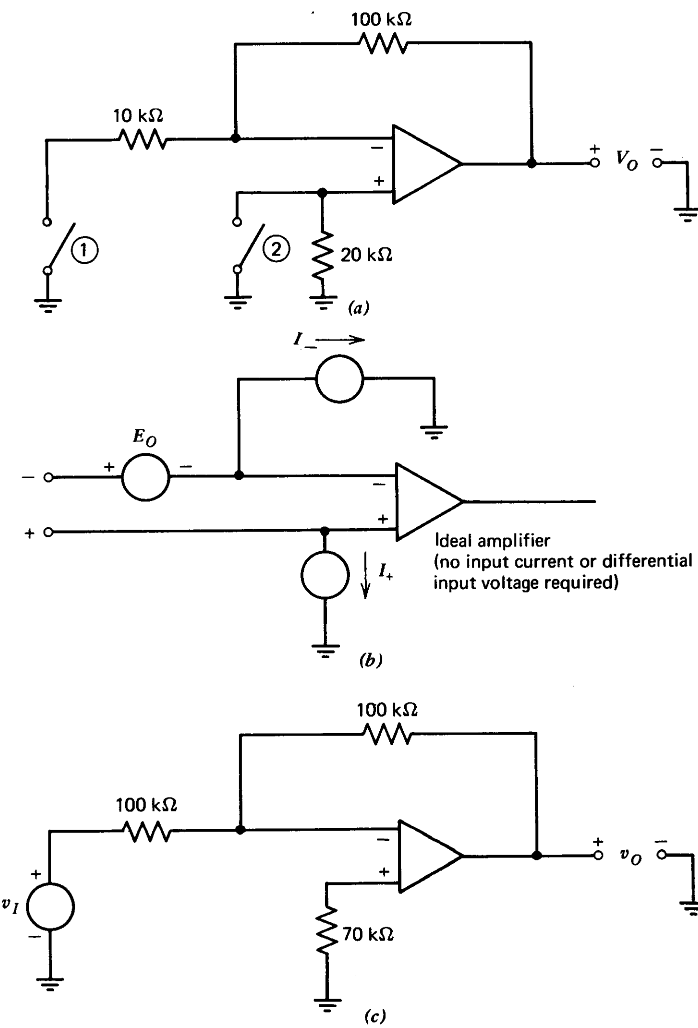


Figure 11.35 (*a*) Test circuit. (*b*) Model. (*c*) Amplifier connection.

+50 mV with zero input voltage in this connection. The amplifier in question has provision for reducing the input offset voltage at one temperature to zero by use of an appropriately connected external potentiometer that effectively changes the magnitude of current sources that load the amplifier input-stage transistors. It is found that by use of an extreme setting of the balance pot it is possible to make the output voltage of the inverter zero for zero input voltage. Discuss possible disadvantages of this method of adjustment. Suggest alternatives likely to yield superior performance.

P11.4

A simplified schematic for an integrated-circuit operational amplifier is shown in Fig. 11.36. Careful open-loop gain measurements indicate a gain of 300,000 at 1 kHz for the uncompensated amplifier and that the first pole in the amplifier transfer function is above this frequency. In the absence of load, the heating attributable to transistor Q_3 and its current-source load raise the temperature of Q_2 0.1° C above that of Q_1 under static conditions with the output at its negative saturation level of -13 volts. Similarly, with the output at its positive saturation level ($+13$ volts) the temperature of transistor Q_1 is eventually raised 0.1° C above that of Q_2. Plot the v_O versus v_I characteristics that result for very slow variations in v_I. Now assume that the chip locations of transistors Q_1 and Q_2 are interchanged. Again plot the v_O versus v_I characteristics. Discuss how these results can complicate measurements of low-frequency open-loop gain.

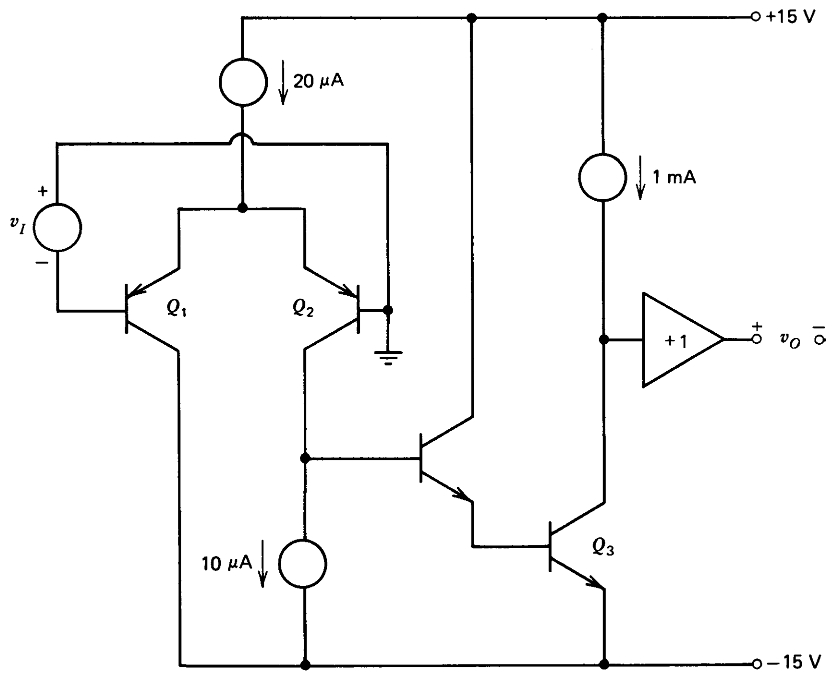


Figure 11.36 Operational amplifier.

P11.5

Integrated-circuit operational amplifiers that use an input stage similar to that of the LM101A (see Section 10.4.1) generally have a high maximum differential input voltage rating. Explain why differential input voltages of approximately 30 volts are possible with this stage compared with the 6-volt maximum level typically specified for a conventional differential amplifier.

P11.6

A low input current operational amplifier has an open-loop transfer function

$$a(s) = \frac{10^6}{(s + 1)(10^{-5}s + 1)}$$

This amplifier is connected to monitor the output current from an ionization gauge. The resultant circuit can be modeled as shown in Fig. 11.37. The capacitance shown at the input of the amplifier includes, in addition to the capacitance of the amplifier itself, the capacitance of the gauge and of the shielded cable used to connect the gauge to the amplifier. Investigate the stability of this circuit. Suggest a method for improving stability.

P11.7

An operational amplifier with high d-c open loop gain and 100-mA output current capacity is connected as shown in Fig. 11.38. Low-frequency measurements indicate an incremental gain $v_o/v_i = 1100$. Explain.

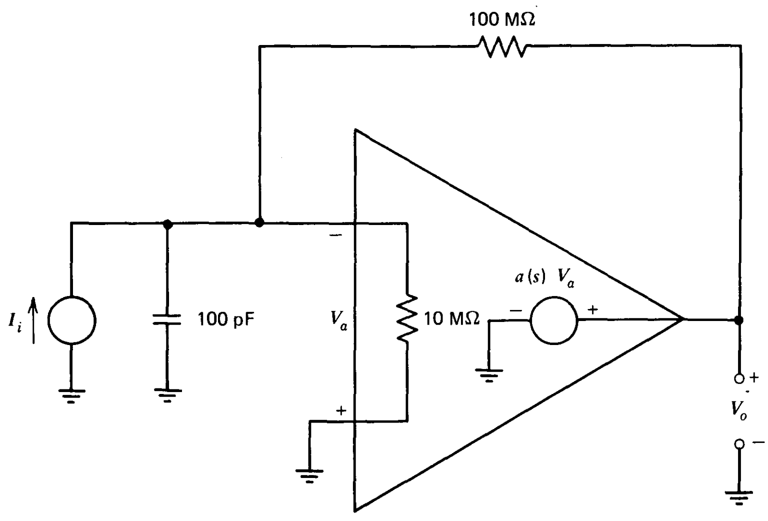


Figure 11.37 Model for operational amplifier connected to ionization gauge.

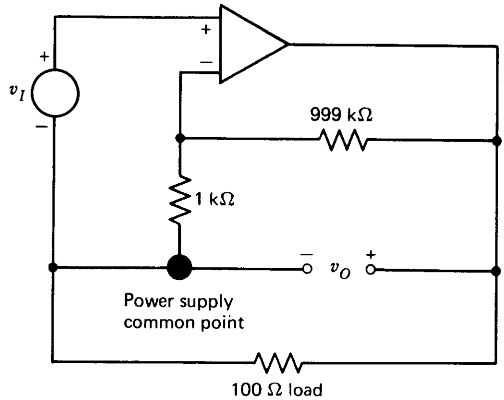


Figure 11.38 Noninverting amplifier connection.

P11.8

Measurements reveal that the dielectric absorption associated with a certain 1-μF capacitor can be modeled as shown in Fig. 11.39. Design a circuit that combines this capacitor with an ideal operational amplifier and any necessary passive components such that the closed-loop transfer function is $-1/s$.

P11.9

A differential connection as shown in Fig. 11.10 is constructed with $Z_1 = Z_3 = 1\ \text{k}\Omega$ and $Z_2 = Z_4 = 10\ \text{k}\Omega$. The operational amplifier has very high d-c open-loop gain and a common-mode rejection ratio of 10^4. Assuming all other operational-amplifier characteristics are ideal, what output voltage results with both inputs equal to one volt? Suggest a modification that raises the common-mode rejection ratio for the connection.

P11.10

An operational amplifier with a d-c open-loop gain of 10^5 is connected as a current source with the topology shown in Fig. 11.14. The resistor

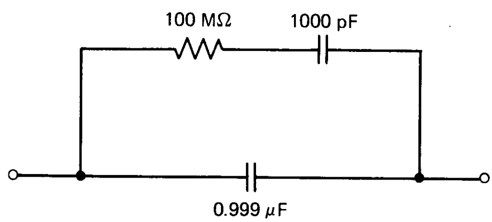


Figure 11.39 Capacitor with dielectric absorption.

value is $R = 10\ \text{k}\Omega$. With an input voltage of $+5$ volts, FET parameters are $y_{fs} = 1$ mmho and $y_{os} = 5\ \mu$mho. (See Fig. 8.19 for a definition of terms.) What is the incremental output resistance of this connection?

P11.11

A Howland current source is constructed as shown in Fig. 11.40. Determine the current I_o as a function of V_a, V_b, V_o, and α. Assume that the offset voltage referred to the input of the amplifier is 5 mV and that the operational amplifier saturates at an output voltage level of ± 10 volts. Select the parameter α to maximize the output current available at zero output voltage subject to the constraint that $|i_O| < 5\ \mu\text{A}$ with $v_A = v_B = 0$.

P11.12

Design a circuit using no inductors that provides a driving-point impedance $Z = -1\ \text{k}\Omega + 10^{-2}s$.

P11.13

A nonlinear lag network is required to compensate a servomechanism. (See Section 6.3.5 for a discussion of this type of network.) The network should have a transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{0.02s + 1}{s + 1}$$

for small input-signal levels. When the magnitude of the voltage across the capacitor exceeds 0.1 volt, the capacitor voltage should be clamped to pre-

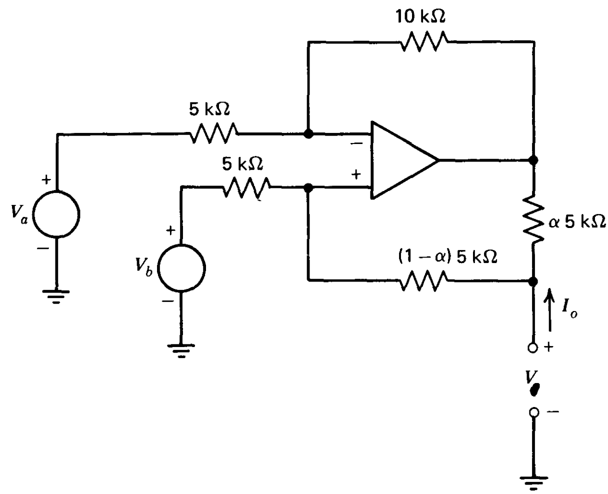


Figure 11.40 Differential current source.

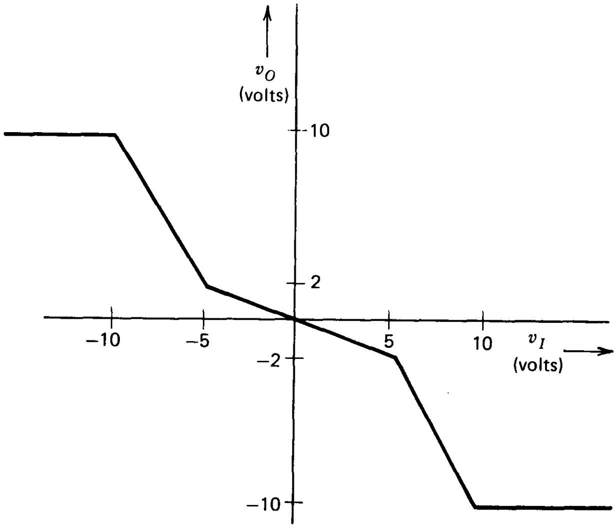


Figure 11.41 Nonlinear transfer characteristics.

vent further increases. Thus the large-signal transfer characteristics will approach $v_O/v_I \simeq 0.02$, independent of frequency.

Design the required network using a capacitor no larger than 5 μF. Provide buffering so that a power amplifier with 1-kΩ input resistance does not load the network appreciably. The capacitor-voltage limiting level for your design should be relatively temperature independent.

P11.14

Design a circuit that provides the transfer characteristics shown in Fig. 11.41. Use a configuration that makes the breakpoint locations well defined and relatively temperature independent. Select resistor values so that operational-amplifier input bias currents of 100 nA do not significantly affect performance and so that the loads applied to the outputs of the amplifiers used are less the 1 mA for any $|v_I| < 15$ volts.

P11.15

Design a circuit that provides an output

$$v_O = \frac{\sqrt{v_X v_Y{}^3}}{10 \text{ volts}}$$

You may assume that both v_X and v_Y are limited to a range of 0 to -10 volts. Assume that any operational amplifiers used can provide undistorted outputs of ± 10 volts. You should design your circuit so that various voltage levels are close to maximum values for maximum input signal levels in order to improve dynamic range. Comment on the temperature stability of your design.

P11.16

A sample-and-hold circuit is built using the topology shown in Fig. 11.34. The open-loop transfer function of the first operational amplifier is

$$a(s) = \frac{10^5}{(0.01s + 1)(5 \times 10^{-8}s + 1)^2}$$

and an LM110 amplifier with a closed-loop bandwidth in excess of 20 MHz is used as the output buffer. The sum of the FET on resistance and the resistor shunting the current-booster transistors is 1 kΩ, and the capacitor value is 1 μF. Investigate the stability of this system under small-signal conditions of operation. Suggest a circuit modification that can be used to improve stability. Comment on the effectiveness of your method under large-signal conditions (with the booster transistors conducting) as well as for linear-region operation.